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Rapid Acquisition of Manufactured Parts (RAMP) Product Data Translation System (RPTS) for Printed Wiring Assemblies (PWA) IDEF0 Activity Model

5. FUNDING NUMBERS
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6. AUTHOR(S)
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7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
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12a. DISTRIBUTION/AVAILABILITY STATEMENT

This document has been approved for public release and sale; its distribution is unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words)*
The IDEF0 models in this release are to show the functional hiearchy and data flow of the RPTS system. Each model shows a box or node to show a system process. Arrows are used to show data inputs and outputs, controls on the process, and the mechanisms which perform the task. The arrows are called ICOMS which is an acronym for Inputs, Controls, Outputs, and Mechanisms as shown in the diagram.

14. SUBJECT TERMS
RAMP, RPTS, CALS, IDEF, PWA, IGES, RTIF

15. NUMBER OF PAGES
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South Carolina Research Authority, 5300 International Blvd., North Charleston, SC 29418

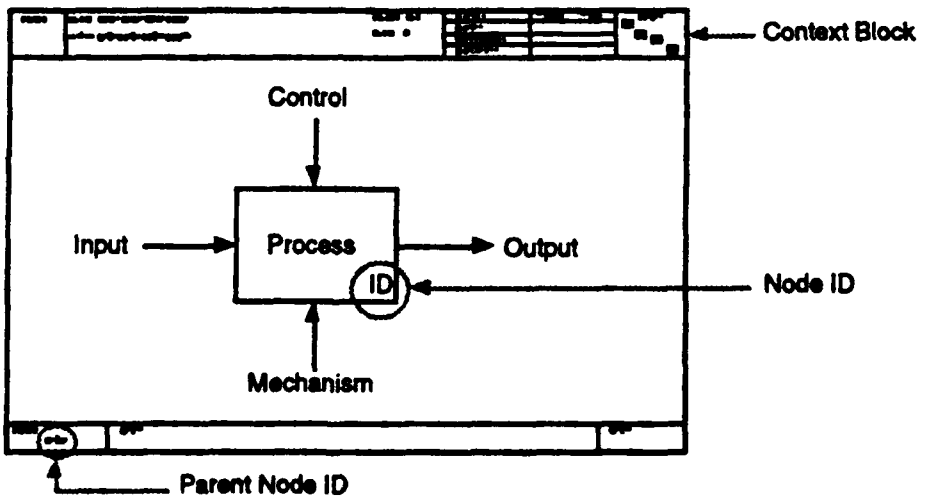
April 10, 1992

-PRELIMINARY-
Rapid Acquisition of Manufactured Parts (RAMP)
Product Data Translation System (RPTS) for PWA
Activity Model

Dear Reviewer,

The RAMP Product Data Translation System for PWA is a CAE system which captures Navy technical drawing packages, verifies the data, and converts them to CALS compliant standards files for use by the RAMP PWA manufacturing system. The standards files used are EDIF, IPC-D-350, IGES, and CCITT-G4. This IDEF0 model shows the functional hierarchy and data flow of the RPTS system. Also shown are system constraints and the mechanisms used for each process. In this model, the mechanisms show how commercial software is used in the system.

The IDEF0 methodology uses a box, or node, to show a system process. Arrows are used to show data inputs and outputs, controls on the process, and the mechanisms which perform the task. The arrows are called ICOMs which is an acronym for Inputs, Controls, Outputs, and Mechanisms as shown in the diagram.



Each node, or process, has an ID in the lower right corner of the box. A node can be decomposed to a subsequent page, showing the processes which occur within that parent node. On the decomposition page, the ID of the parent node is shown in the lower left corner of the page. The position of the decomposed node, on the parent page, is shown in the Context Block.

For more information on the RPTS PWA, you may request the RAMP document "RAMP Product Data Translation System Functional Specification for the RAMP/RTIF Program." I would appreciate any interest you have in this system or comments on the model. Please send your comments and requests to: Rob Fletcher, c/o SCRA/ADL, Trident Research Center, 5300 International Blvd., North Charleston, SC 29418/email: fletcher@trc.scra.org/phone: (803)760-3331/fax: (803)760-3482.

USED AT:	AUTHOR: Rob Fletcher	DATE: 4/7/92	X	WORKING	READER DATE	CONTEXT:
RAMP	PROJECT: RAMP Product Data Translation System (RPTS) for Printed Wiring Assemblies (PWA)	REV: 2		DRAFT		Top
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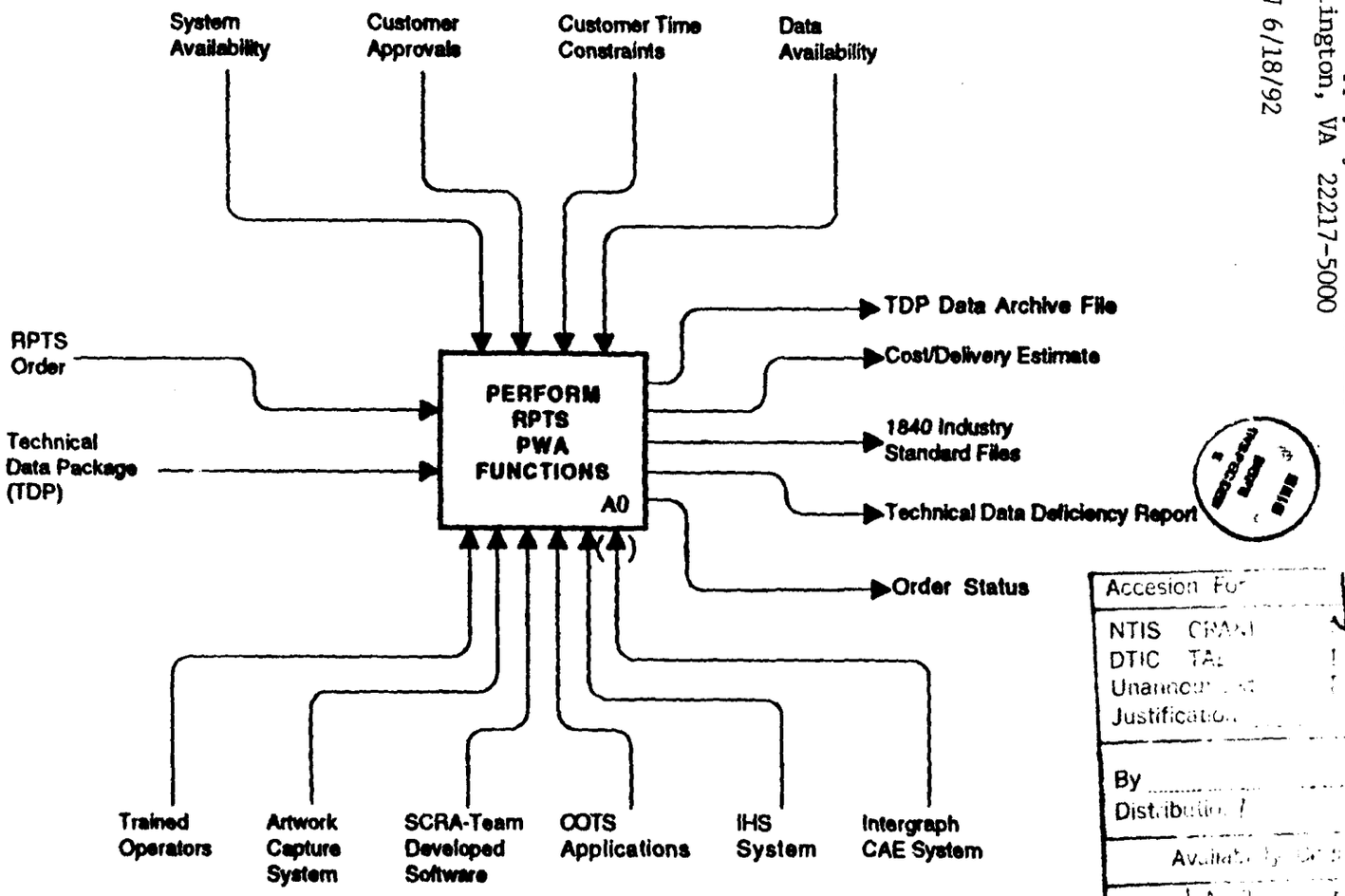

Viewpoint: SCRA RPTS PWA Development Team
Purpose: System Analysis, Design, and Presentation

Statement A per telecon Lorna Esten
Naval Supply Systems Command SUP 642
Arlington, VA 22217-5000
NWW 6/18/92

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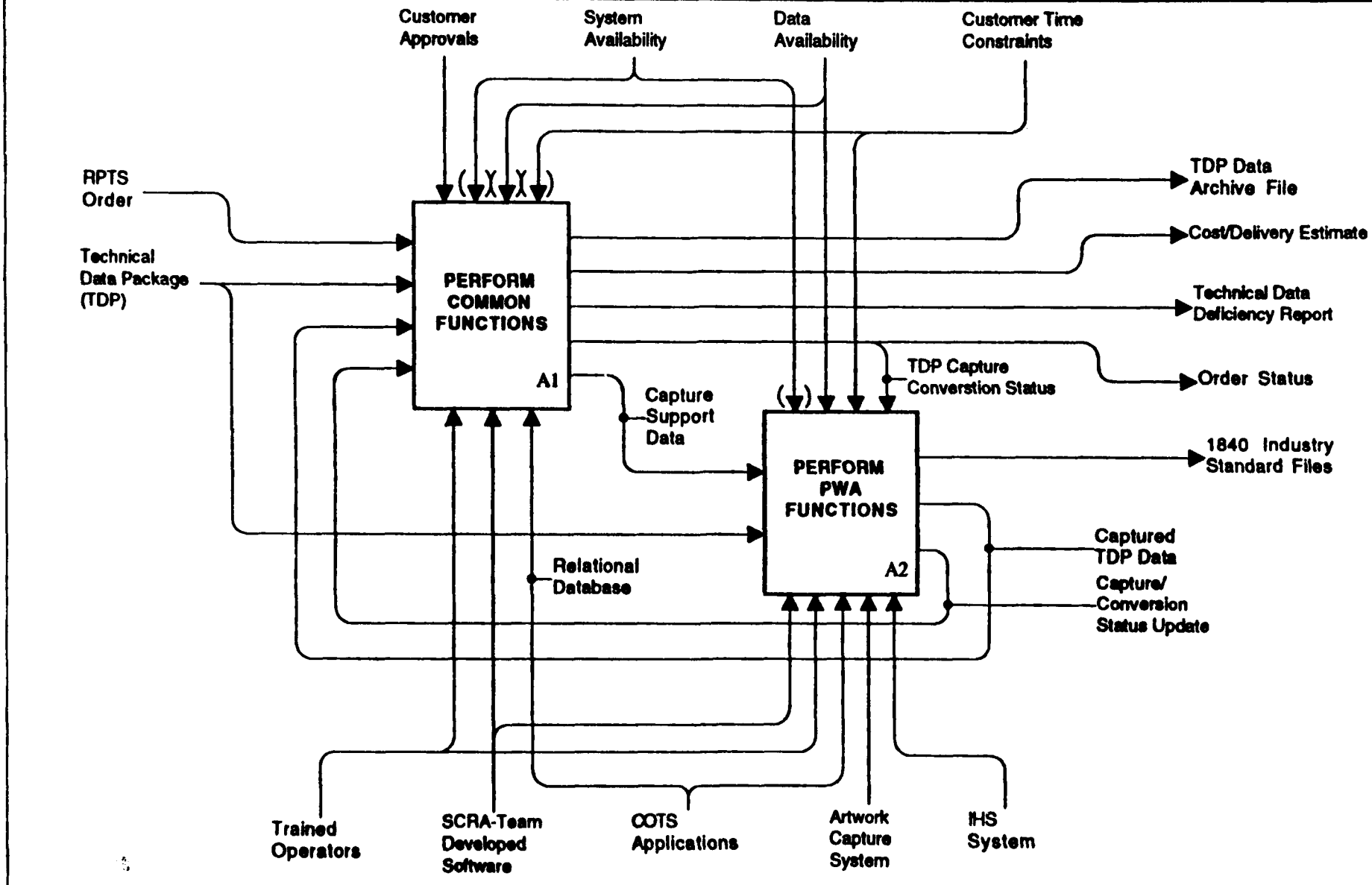
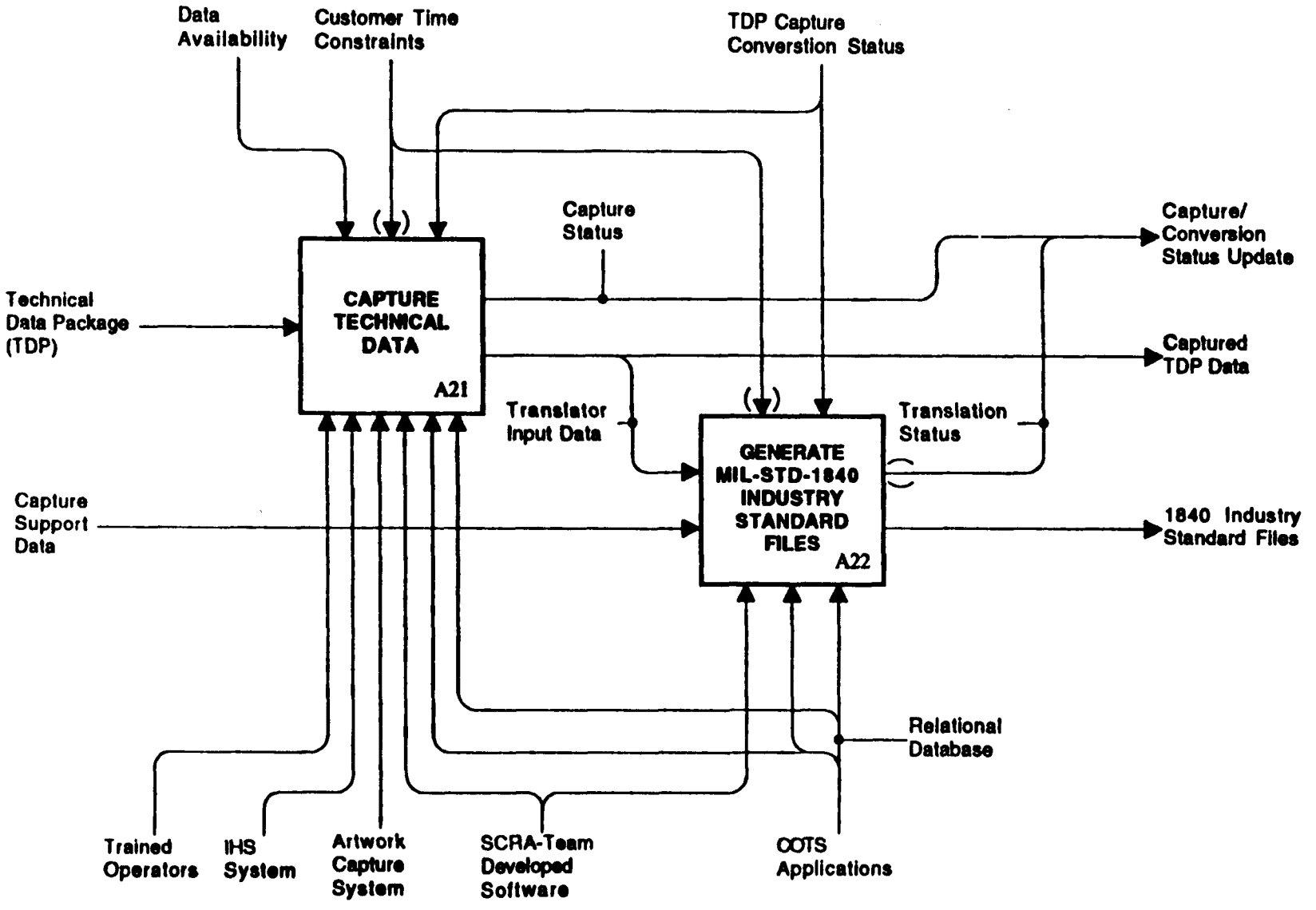
NODE: A-0	TITLE: RAMP Product Data Translation System for PWA - Activity Model	NUMBER:

USED AT:	AUTHOR: Rob Fletcher	DATE: 4/7/92	X	WORKING	READER DATE	CONTEXT:
RAMP	PROJECT: RAMP Product Data Translation System (RPTS) for Printed Wiring Assemblies (PWA)	REV: 2		DRAFT		■
	NOTES: 1 2 3 4 5 6 7 8 9 10			RECOMMENDED		
				PUBLICATION		



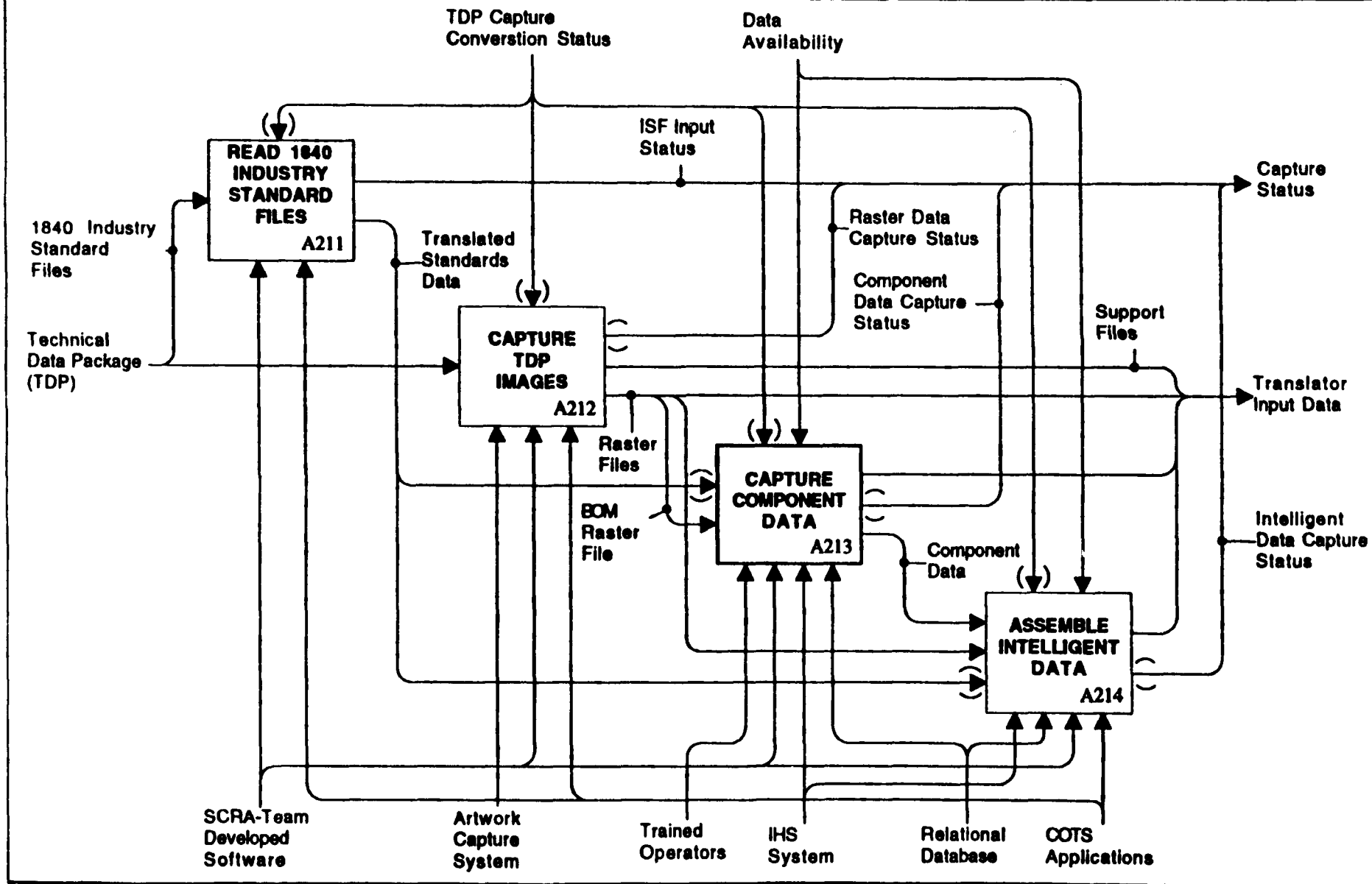
NODE: A0	TITLE: PERFORM RPTS PWA FUNCTIONS	NUMBER:

USED AT:	AUTHOR: Rob Fletcher	DATE: 4/7/92	X	WORKING	READER DATE	CONTEXT:
RAMP	PROJECT: RAMP Product Data Translation System (RPTS) for Printed Wiring Assemblies (PWA)	REV: 2		DRAFT		
	NOTES: 1 2 3 4 5 6 7 8 9 10			RECOMMENDED		
				PUBLICATION		



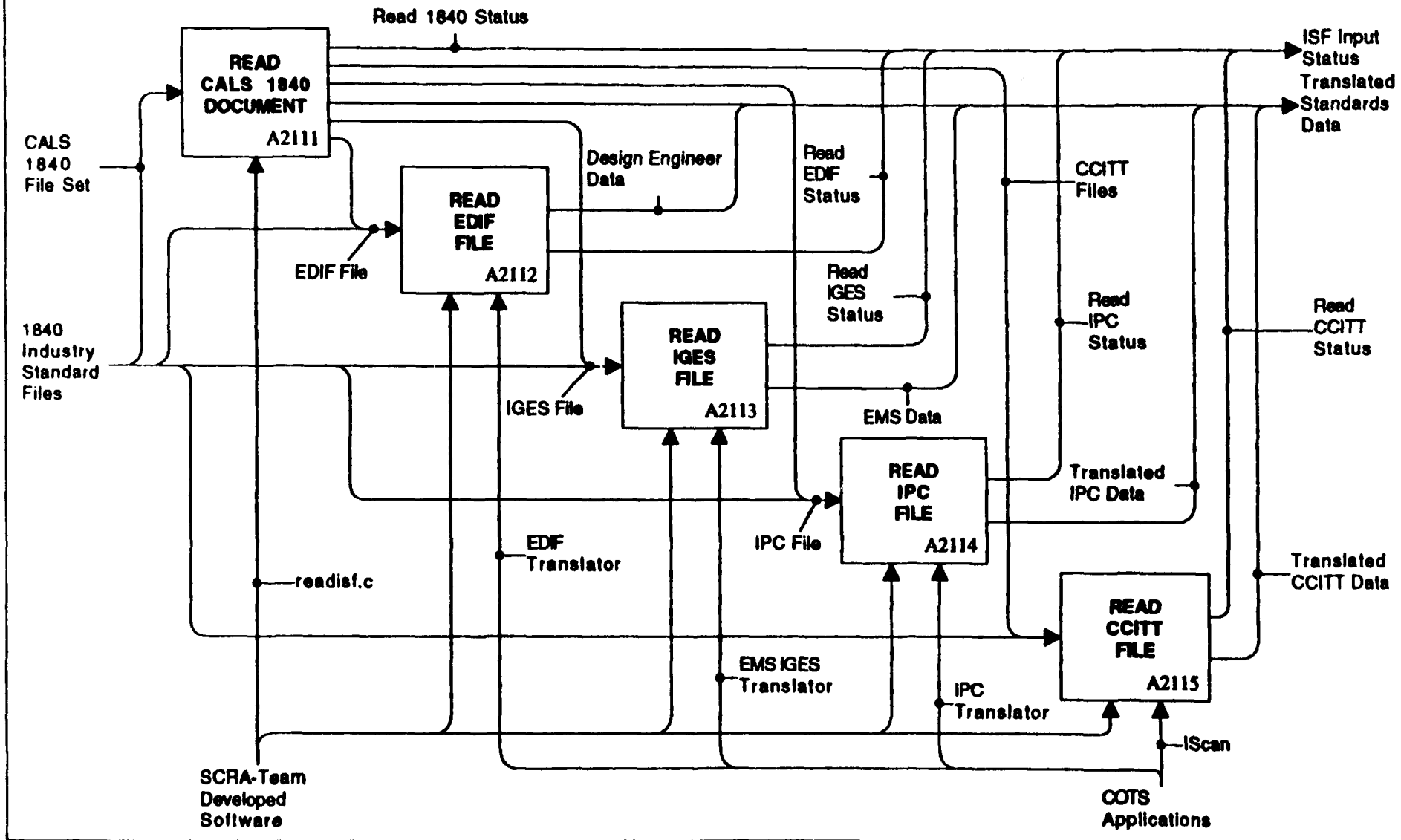
NODE: A2	TITLE: PERFORM PWA FUNCTIONS	NUMBER:

USED AT:	AUTHOR: Rob Fletcher	DATE: 4/7/92	X	WORKING	READER DATE	CONTEXT:
RAMP	PROJECT: RAMP Product Data Translation System (RPTS) for Printed Wiring Assemblies (PWA)	REV: 2		DRAFT		■ □
	NOTES: 1 2 3 4 5 6 7 8 9 10			RECOMMENDED		
				PUBLICATION		



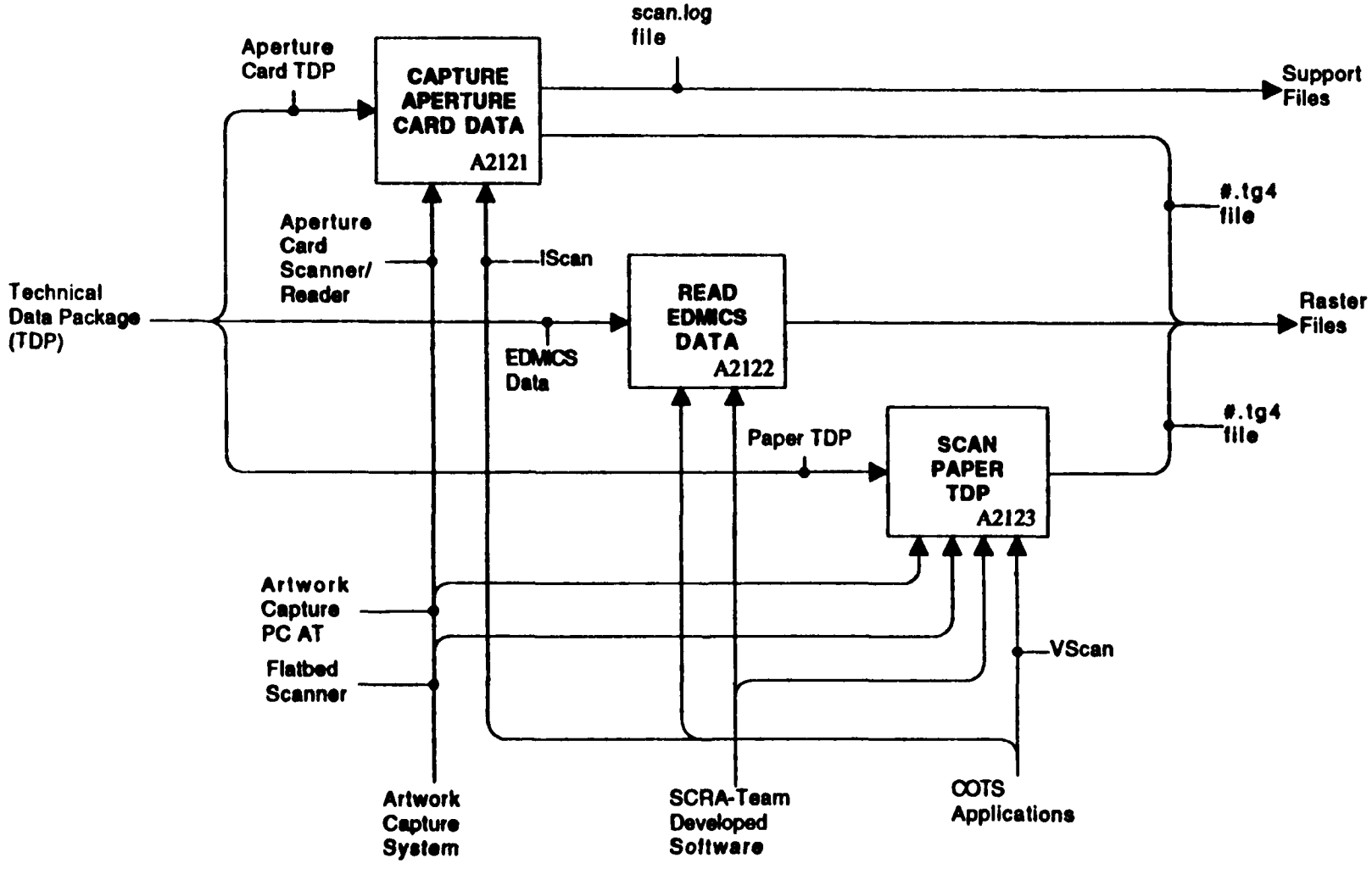
NODE: A21	TITLE: CAPTURE TECHNICAL DATA	NUMBER:

USED AT:	AUTHOR: Rob Fletcher	DATE: 4/7/92	X	WORKING	READER DATE	CONTEXT:
RAMP	PROJECT: RAMP Product Data Translation System (RPTS) for Printed Wiring Assemblies (PWA)	REV: 2		DRAFT		
	NOTES: 1 2 3 4 5 6 7 8 9 10			RECOMMENDED		
				PUBLICATION		



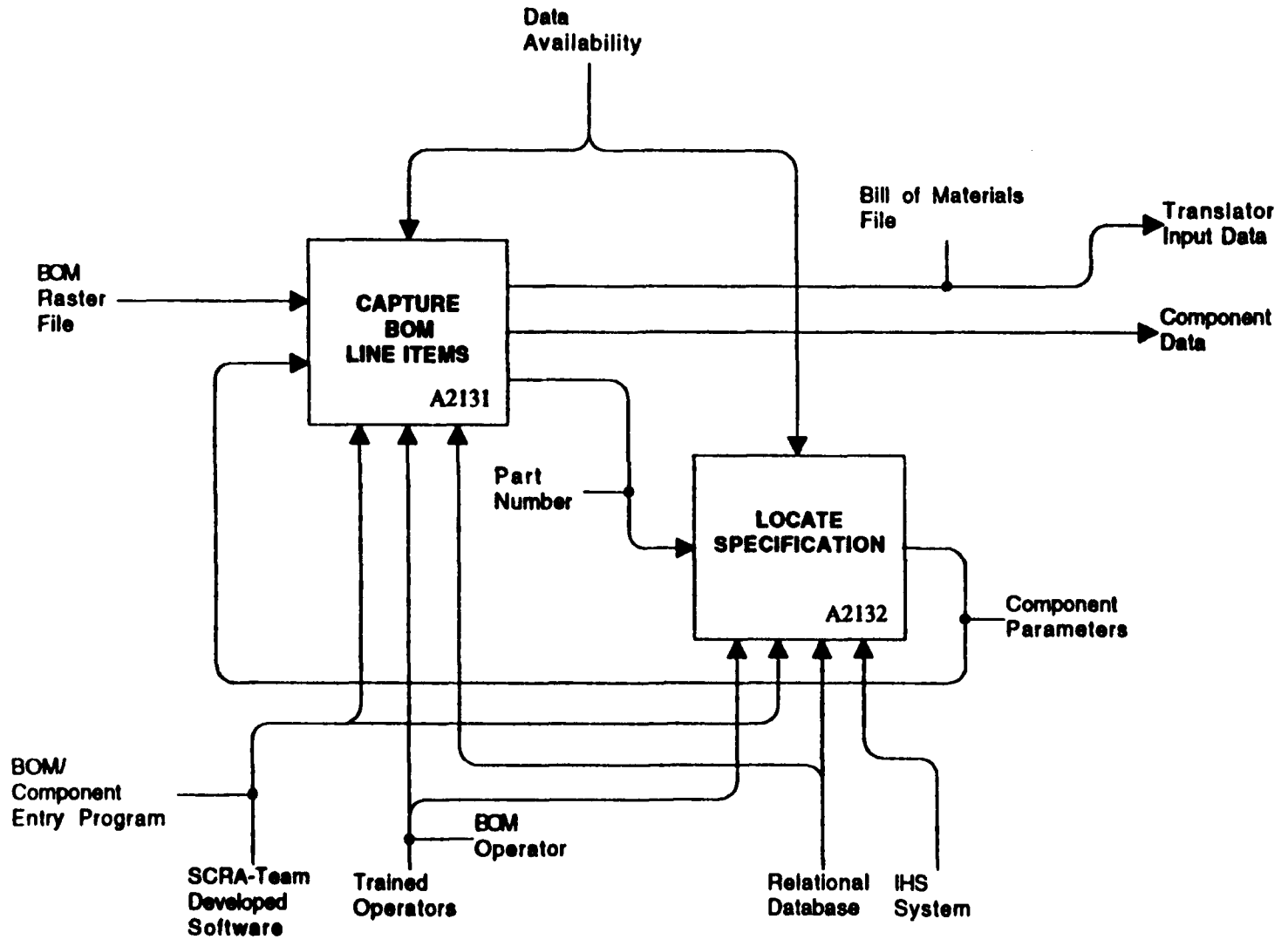
NODE: A211	TITLE: READ 1840 INDUSTRY STANDARD FILES	NUMBER:

USED AT:	AUTHOR: Rob Fletcher	DATE: 4/7/92	X	WORKING	READER DATE	CONTEXT:
RAMP	PROJECT: RAMP Product Data Translation System (RPTS) for Printed Wiring Assemblies (PWA)	REV: 2		DRAFT		
	NOTES: 1 2 3 4 5 6 7 8 9 10			RECOMMENDED		
				PUBLICATION		



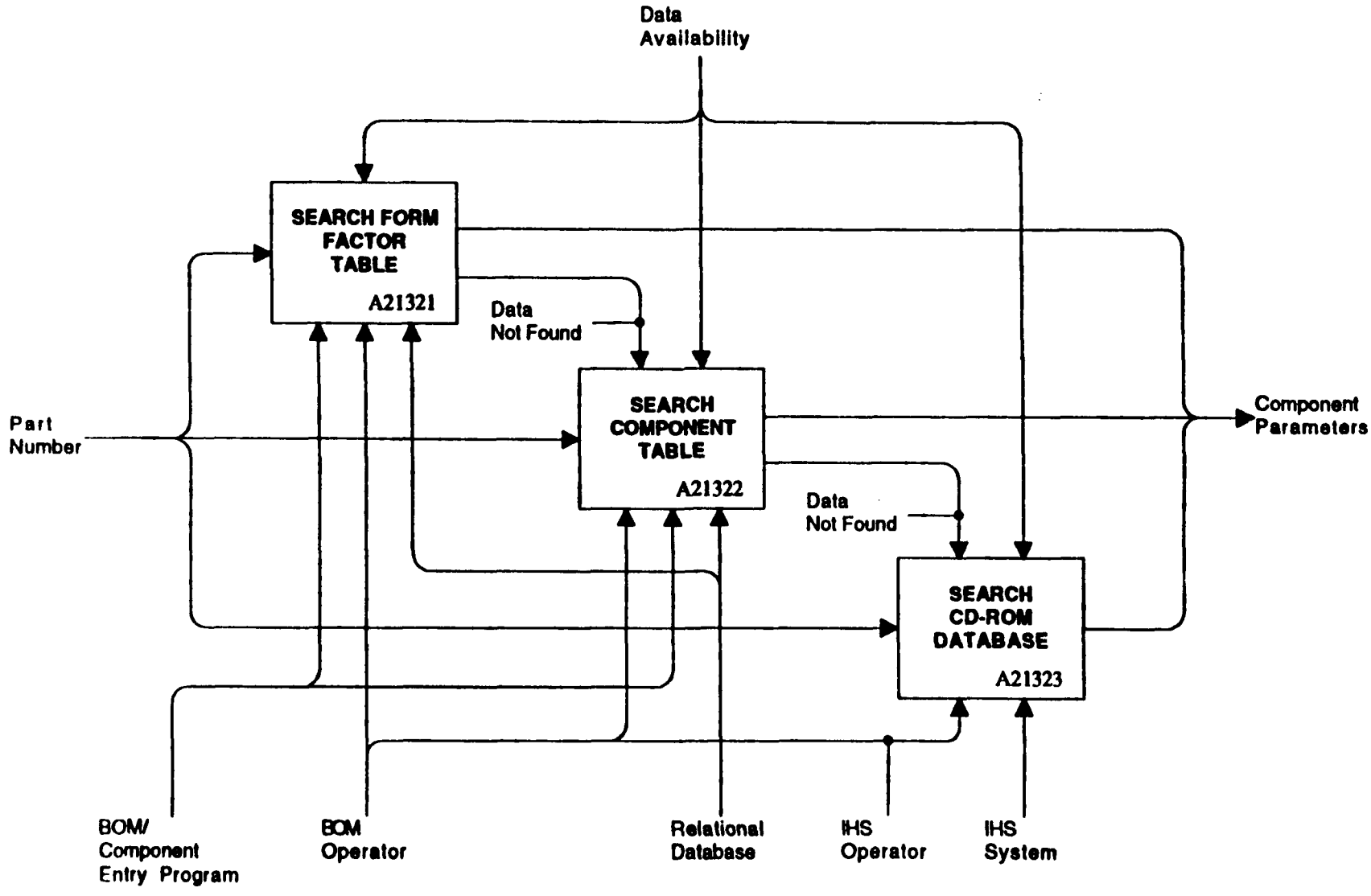
NODE: A212	TITLE: CAPTURE TDP IMAGES	NUMBER:

USED AT:	AUTHOR: Rob Fletcher	DATE: 4/7/92	X	WORKING	READER DATE	CONTEXT:
RAMP	PROJECT: RAMP Product Data Translation System (RPTS) for Printed Wiring Assemblies (PWA)	REV: 2		DRAFT		
	NOTES: 1 2 3 4 5 6 7 8 9 10			RECOMMENDED		
				PUBLICATION		



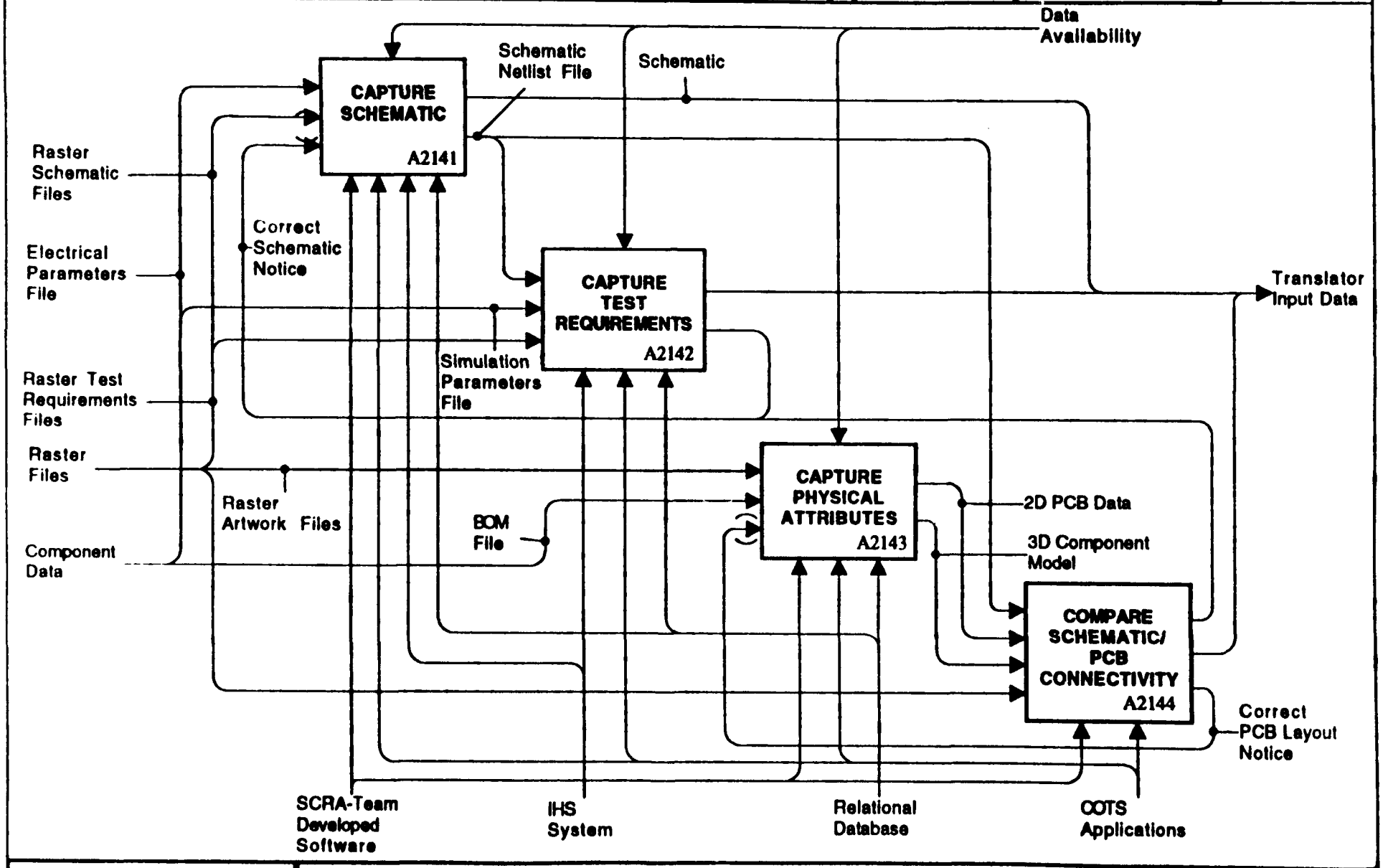
NODE: A213	TITLE: CAPTURE COMPONENT DATA	NUMBER:

USED AT:	AUTHOR: Rob Fletcher	DATE: 4/7/92	X	WORKING	READER DATE	CONTEXT:
RAMP	PROJECT: RAMP Product Data Translation System (RPTS) for Printed Wiring Assemblies (PWA)	REV: 2		DRAFT		
	NOTES: 1 2 3 4 5 6 7 8 9 10			RECOMMENDED		
				PUBLICATION		



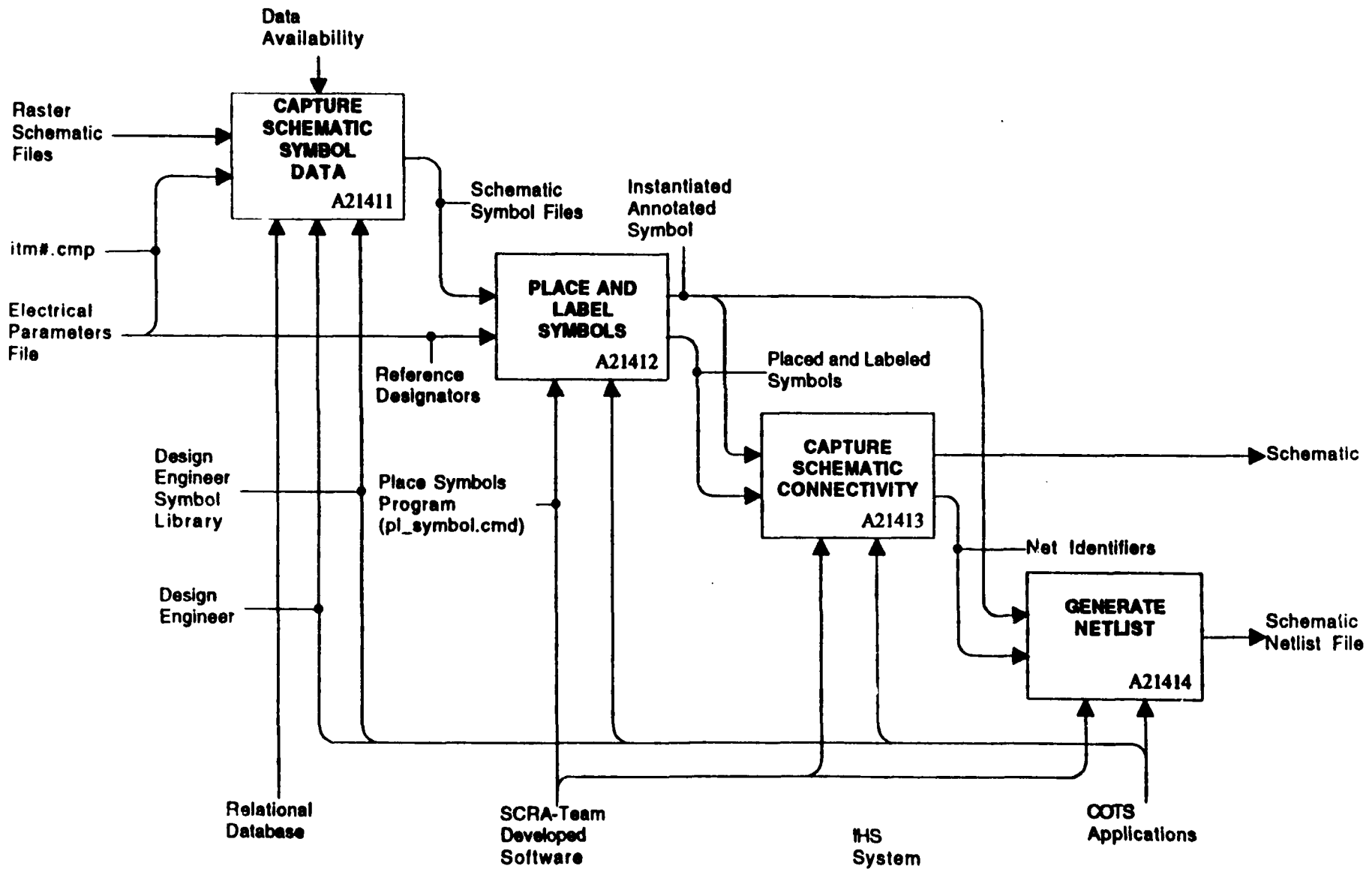
NODE: A2132	TITLE: LOCATE SPECIFICATION	NUMBER:

USED AT:	AUTHOR: Rob Fletcher	DATE: 4/7/92	X	WORKING	READER DATE	CONTEXT:
RAMP	PROJECT: RAMP Product Data Translation System (RPTS) for Printed Wiring Assemblies (PWA)	REV: 2		DRAFT		
	NOTES: 1 2 3 4 5 6 7 8 9 10			RECOMMENDED		
				PUBLICATION		



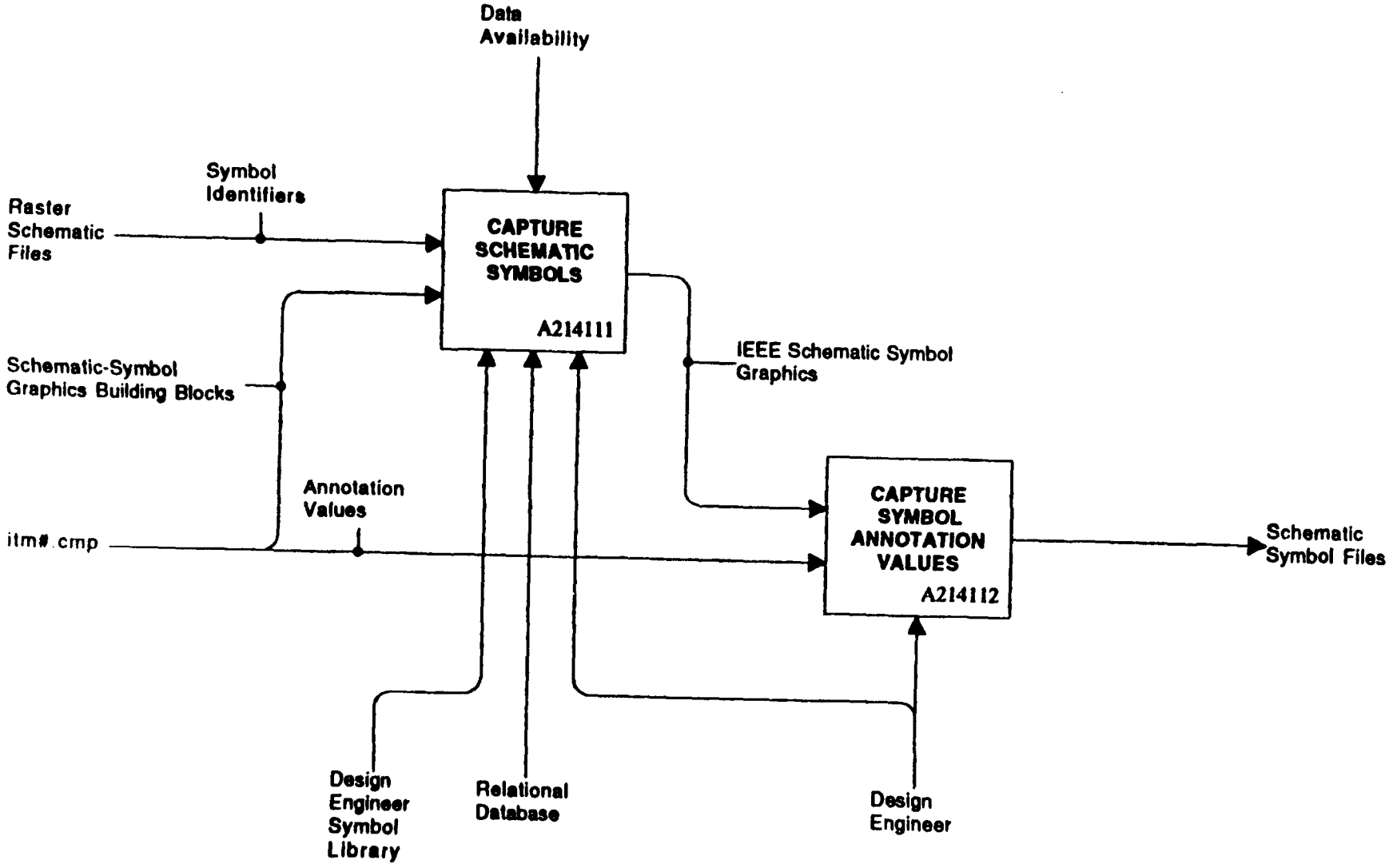
NODE: A214	TITLE: ASSEMBLE INTELLIGENT DATA	NUMBER:

USED AT:	AUTHOR: Rob Fletcher	DATE: 4/7/92	X	WORKING	READER DATE	CONTEXT:
RAMP	PROJECT: RAMP Product Data Translation System (RPTS) for Printed Wiring Assemblies (PWA)	REV: 2		DRAFT		
	NOTES: 1 2 3 4 5 6 7 8 9 10			RECOMMENDED		
				PUBLICATION		



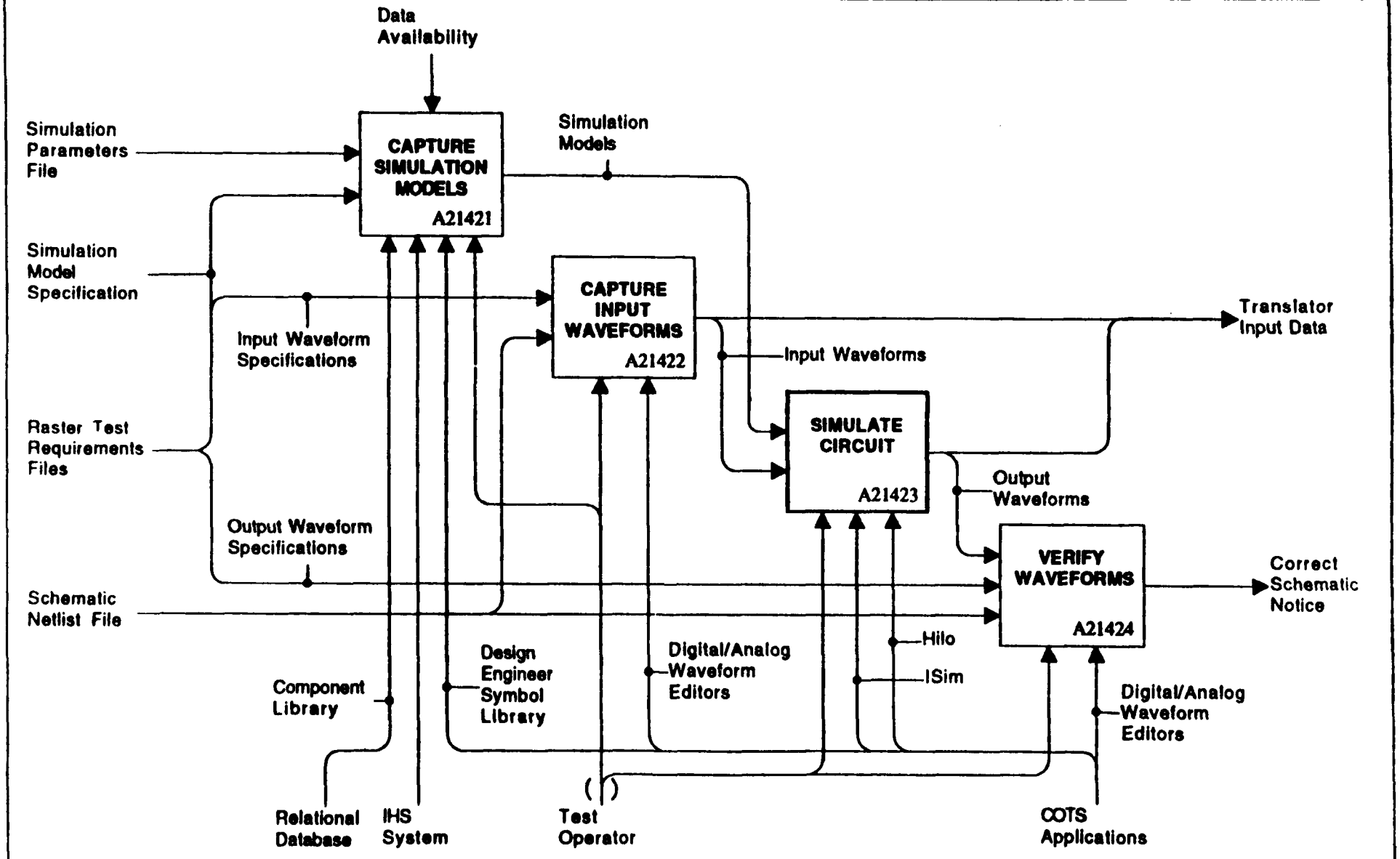
NODE: A2141	TITLE: CAPTURE SCHEMATIC	NUMBER:

USED AT:	AUTHOR: Rob Fletcher	DATE: 4/7/92	X	WORKING	READER DATE	CONTEXT:
RAMP	PROJECT: RAMP Product Data Translation System (RAMPS) for Printed Wiring Assemblies (PWA)	REV: 2		DRAFT		
	NOTES: 1 2 3 4 5 6 7 8 9 10			RECOMMENDED		
				PUBLICATION		



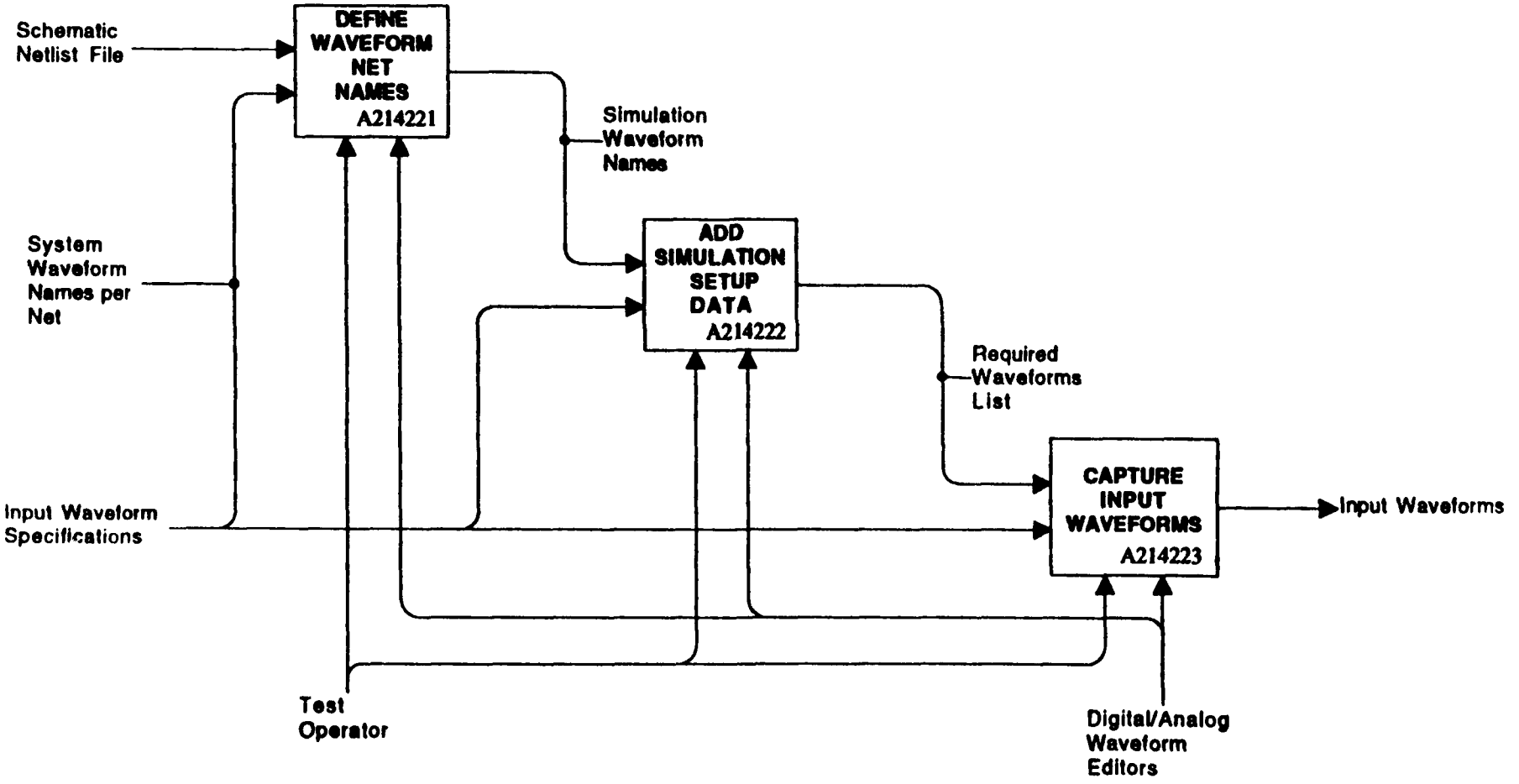
NODE: A21411	TITLE: CAPTURE SCHEMATIC SYMBOL DATA	NUMBER:

USED AT:	AUTHOR: Rob Fletcher	DATE: 4/7/92	X	WORKING	READER DATE	CONTEXT:
RAMP	PROJECT: RAMP Product Data Translation System (RPTS) for Printed Wiring Assemblies (PWA)	REV: 2		DRAFT		
	NOTES: 1 2 3 4 5 6 7 8 9 10			RECOMMENDED		
				PUBLICATION		



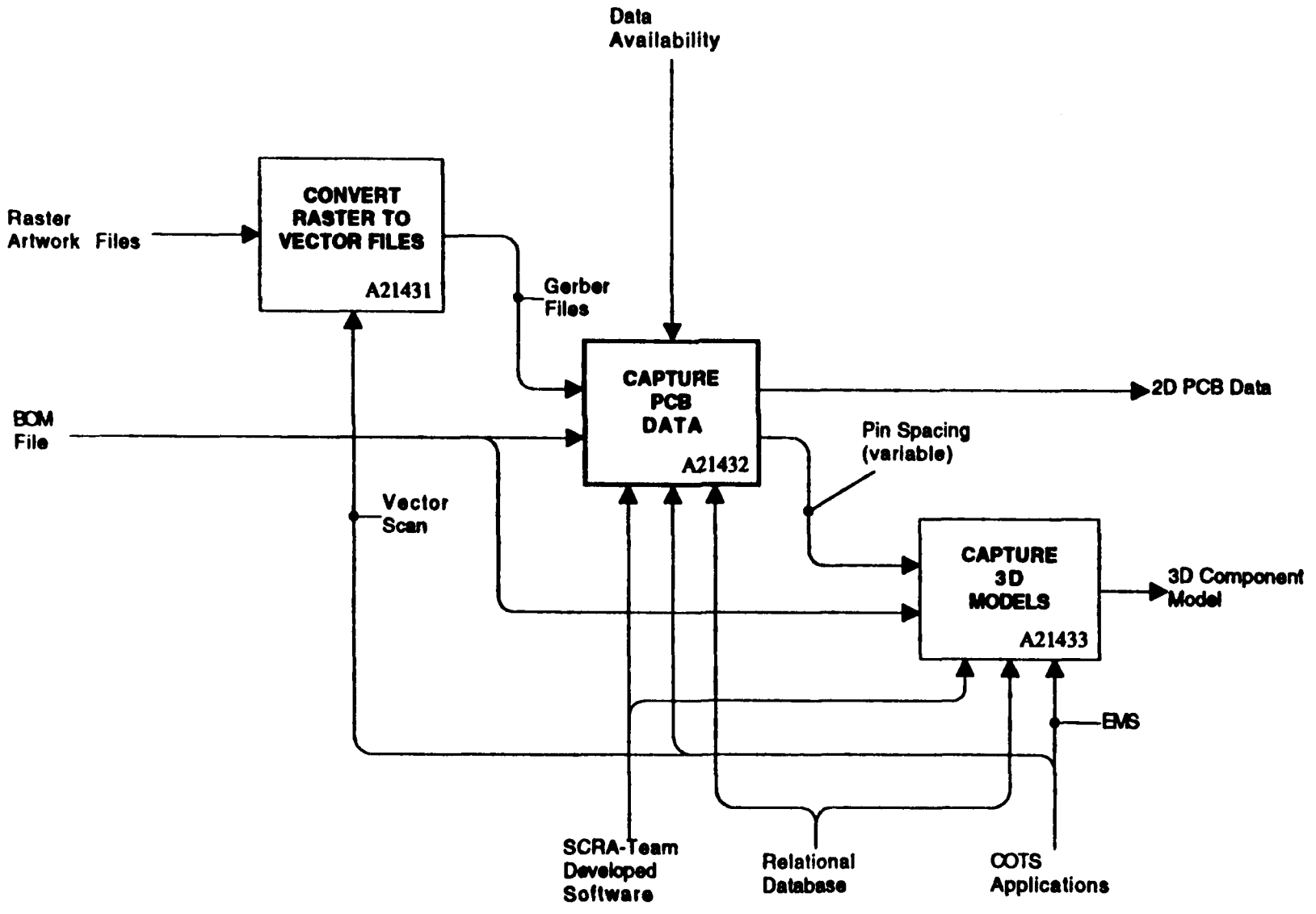
NODE: A2142	TITLE: CAPTURE TEST REQUIREMENTS	NUMBER:

USED AT:	AUTHOR: Rob Fletcher	DATE: 4/7/92	X	WORKING	READER DATE	CONTEXT:
RAMP	PROJECT: RAMP Product Data Translation System (RPTS) for Printed Wiring Assemblies (PWA)	REV: 2		DRAFT		
	NOTES: 1 2 3 4 5 6 7 8 9 10			RECOMMENDED		
				PUBLICATION		



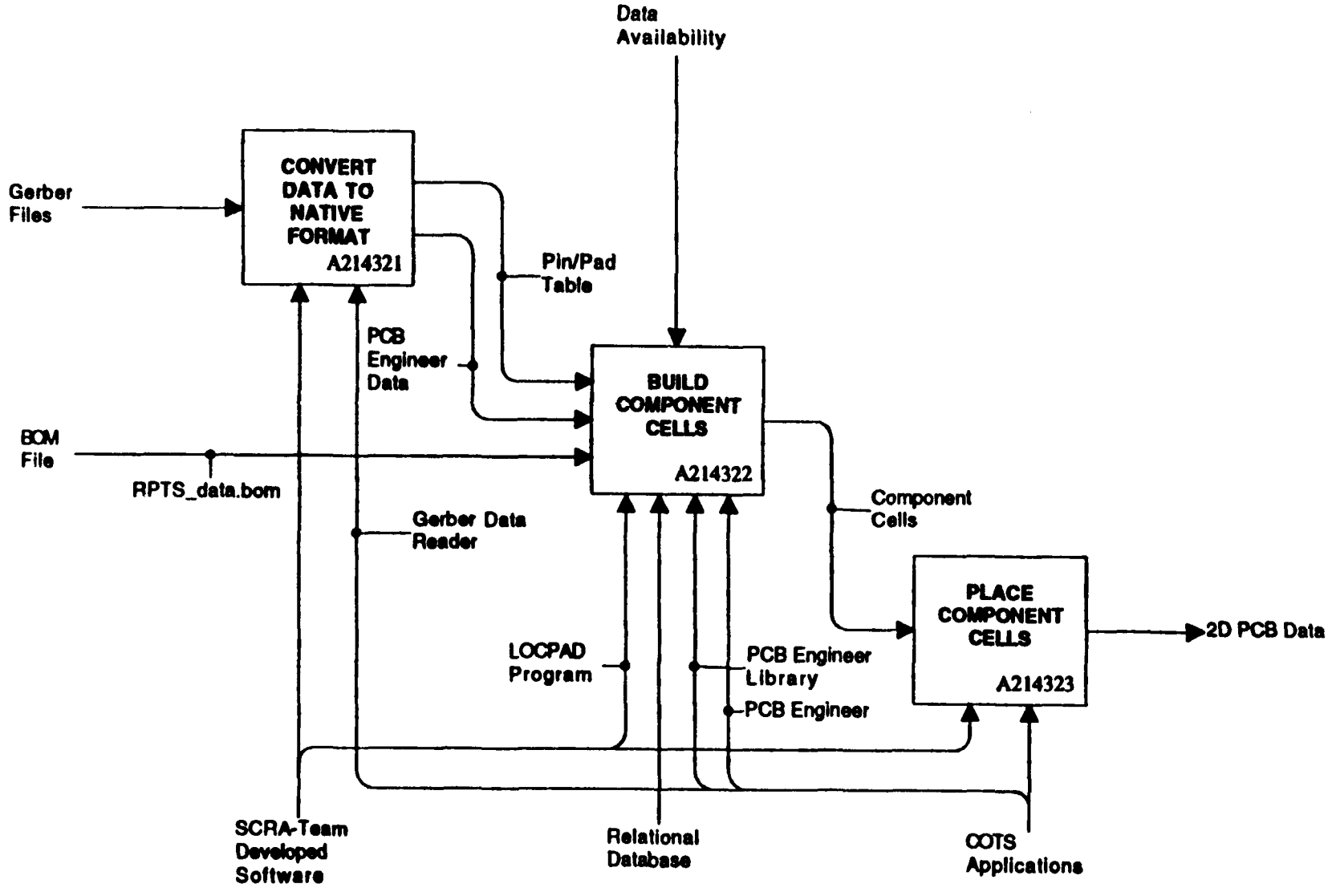
NODE: A21422	TITLE: CAPTURE INPUT WAVEFORMS	NUMBER:

USED AT:	AUTHOR: Rob Fletcher	DATE: 4/7/92	X	WORKING	READER DATE	CONTEXT:
RAMP	PROJECT: RAMP Product Data Translation System (RPTS) for Printed Wiring Assemblies (PWA)	REV: 2		DRAFT		
	NOTES: 1 2 3 4 5 6 7 8 9 10			RECOMMENDED		
				PUBLICATION		



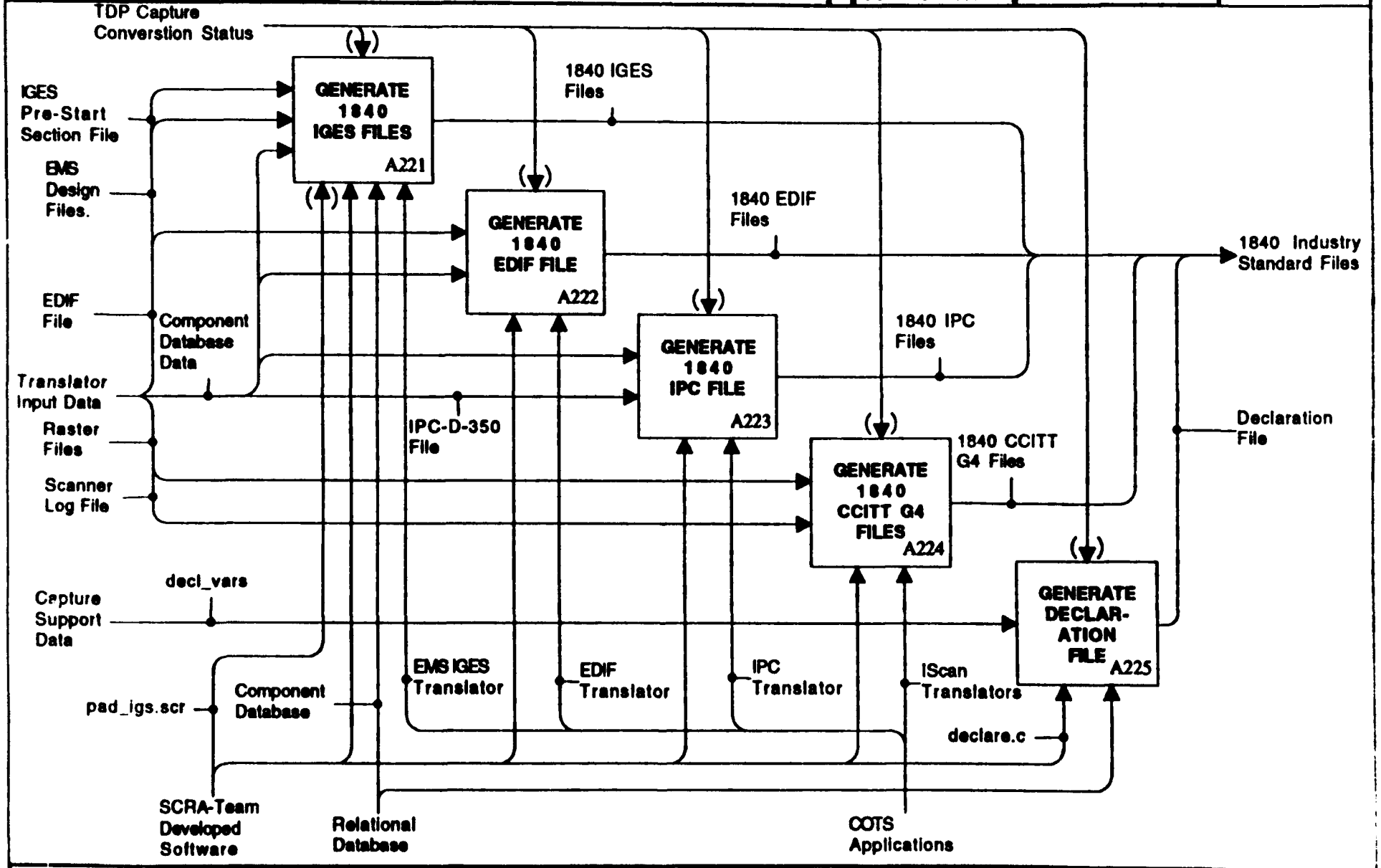
NODE: A2143	TITLE: CAPTURE PHYSICAL ATTRIBUTES	NUMBER:

USED AT:	AUTHOR: Rob Fletcher	DATE: 4/7/92	X	WORKING	READER	DATE	CONTEXT:
RAMP	PROJECT: RAMP Product Data Translation System (RPTS) for Printed Wiring Assemblies (PWA)	REV: 2		DRAFT			
	NOTES: 1 2 3 4 5 6 7 8 9 10			RECOMMENDED			
				PUBLICATION			



NODE: A21432	TITLE: CAPTURE PCB DATA	NUMBER:

USED AT:	AUTHOR: Rob Fletcher	DATE: 4/7/92	X	WORKING	READER	DATE	CONTEXT:
RAMP	PROJECT: RAMP Product Data Translation System (RPTS) for Printed Wiring Assemblies (PWA)	REV: 2		DRAFT			☐ ■
	NOTES: 1 2 3 4 5 6 7 8 9 10			RECOMMENDED			
				PUBLICATION			



NODE: A22	TITLE: GENERATE MIL-STD-1840 INDUSTRY STANDARD FILES	NUMBER:

USED AT:	AUTHOR: Rob Fletcher				
RAMP	PROJECT: RAMP Product Data Translation System (RPTS) for Printed Wiring Assemblies (PWA)	DATE: 4/7/92 REV: 2	X	WORKING	READER DATE
	NOTES: 1 2 3 4 5 6 7 8 9 10			DRAFT	
				RECOMMENDED	
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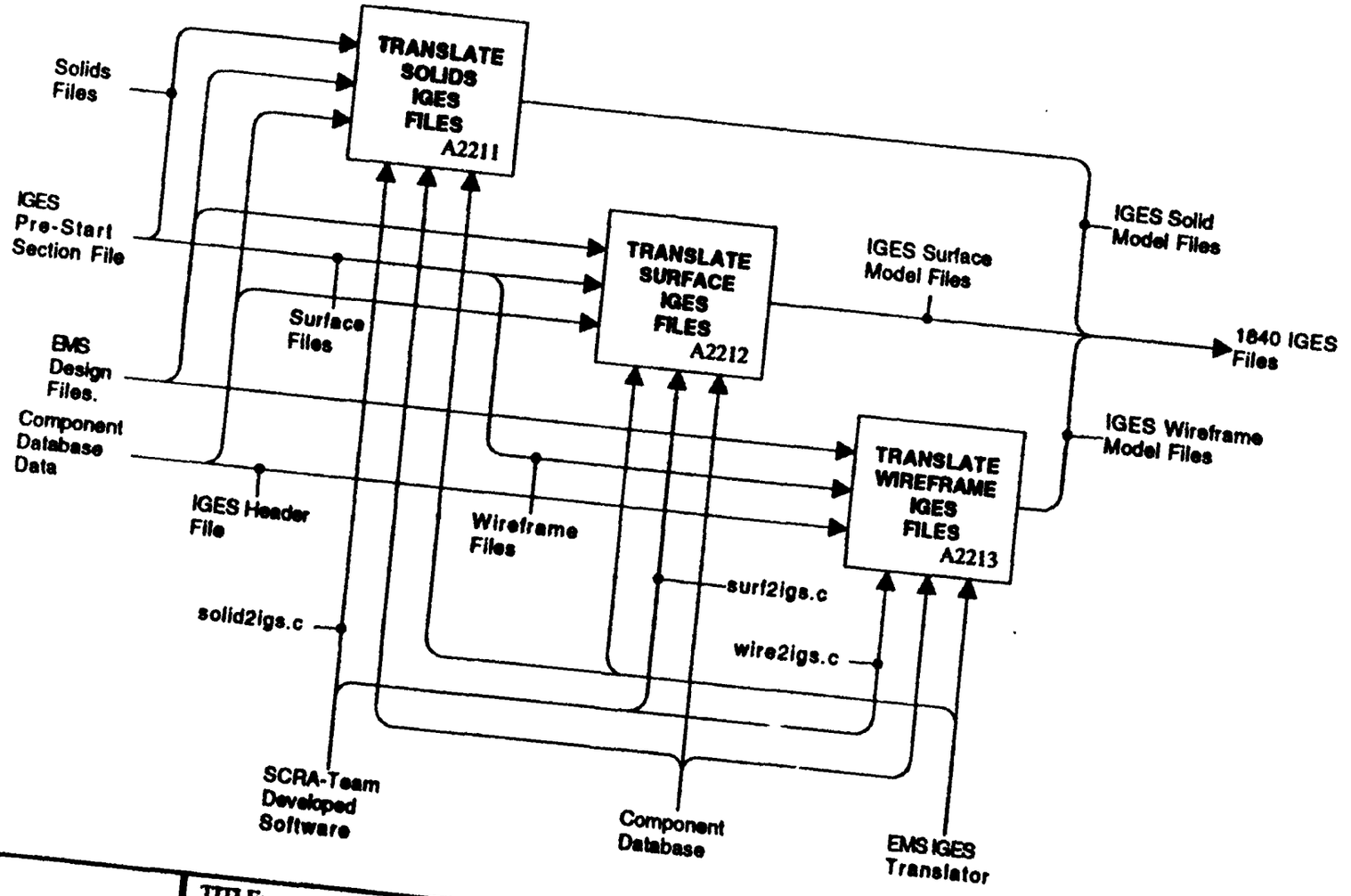
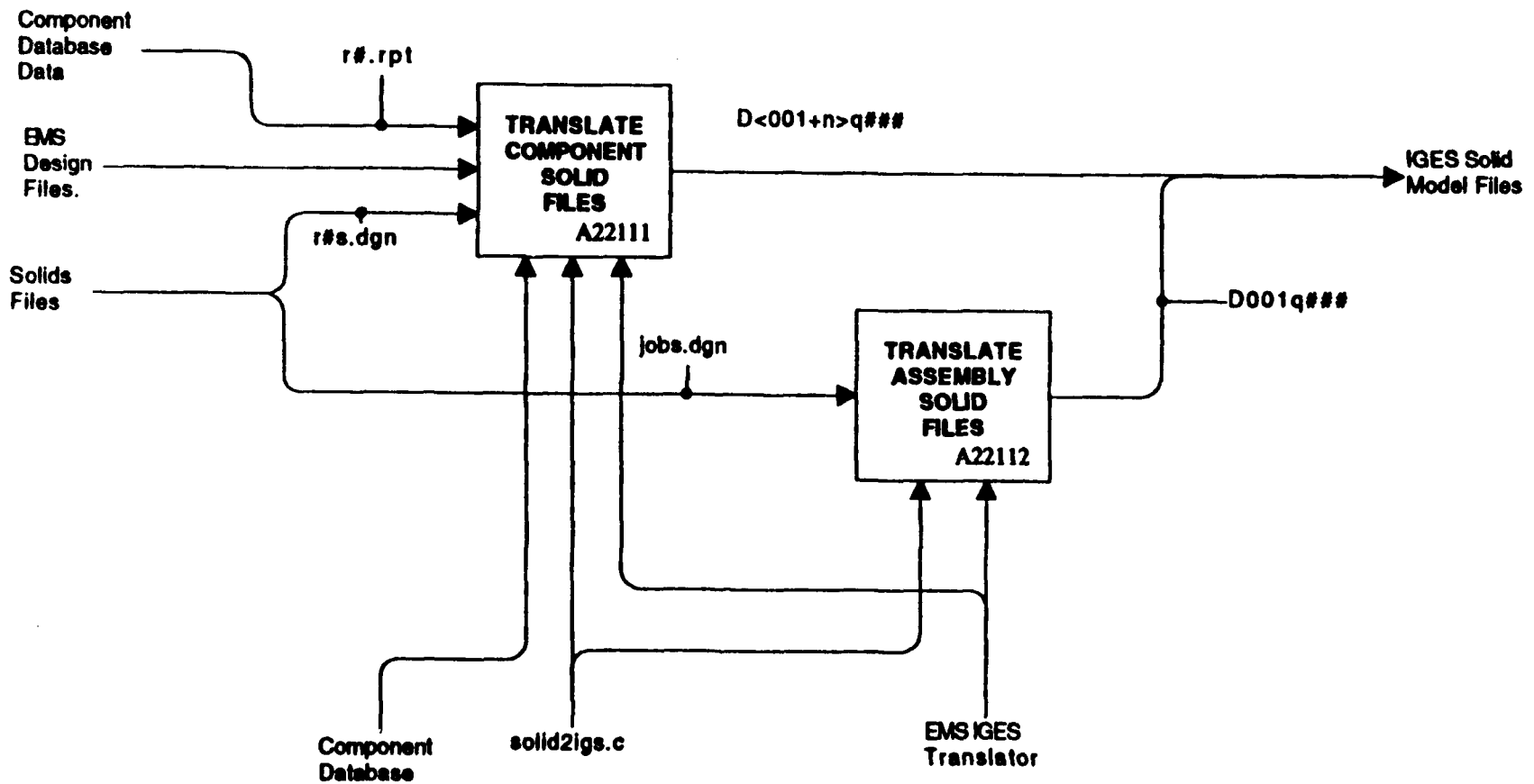
CONTEXT:



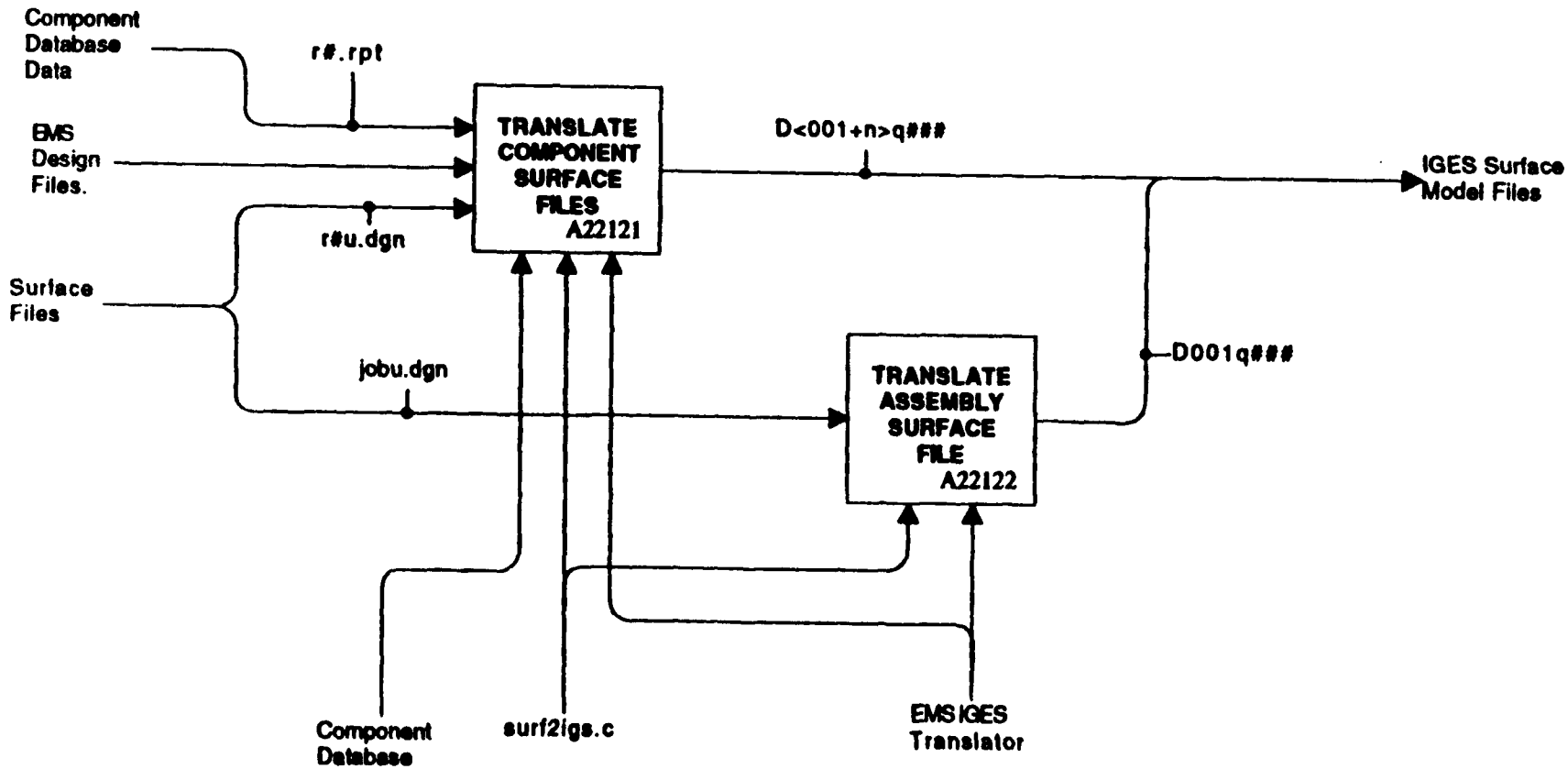
NODE: A221	TITLE: GENERATE 1840 IGES FILES	NUMBER:

USED AT:	AUTHOR: Rob Fletcher	DATE: 4/7/92	X	WORKING	READER DATE	CONTEXT:
RAMP	PROJECT: RAMP Product Data Translation System (RPTS) for Printed Wiring Assemblies (PWA)	REV: 2		DRAFT		
	NOTES: 1 2 3 4 5 6 7 8 9 10			RECOMMENDED		
				PUBLICATION		



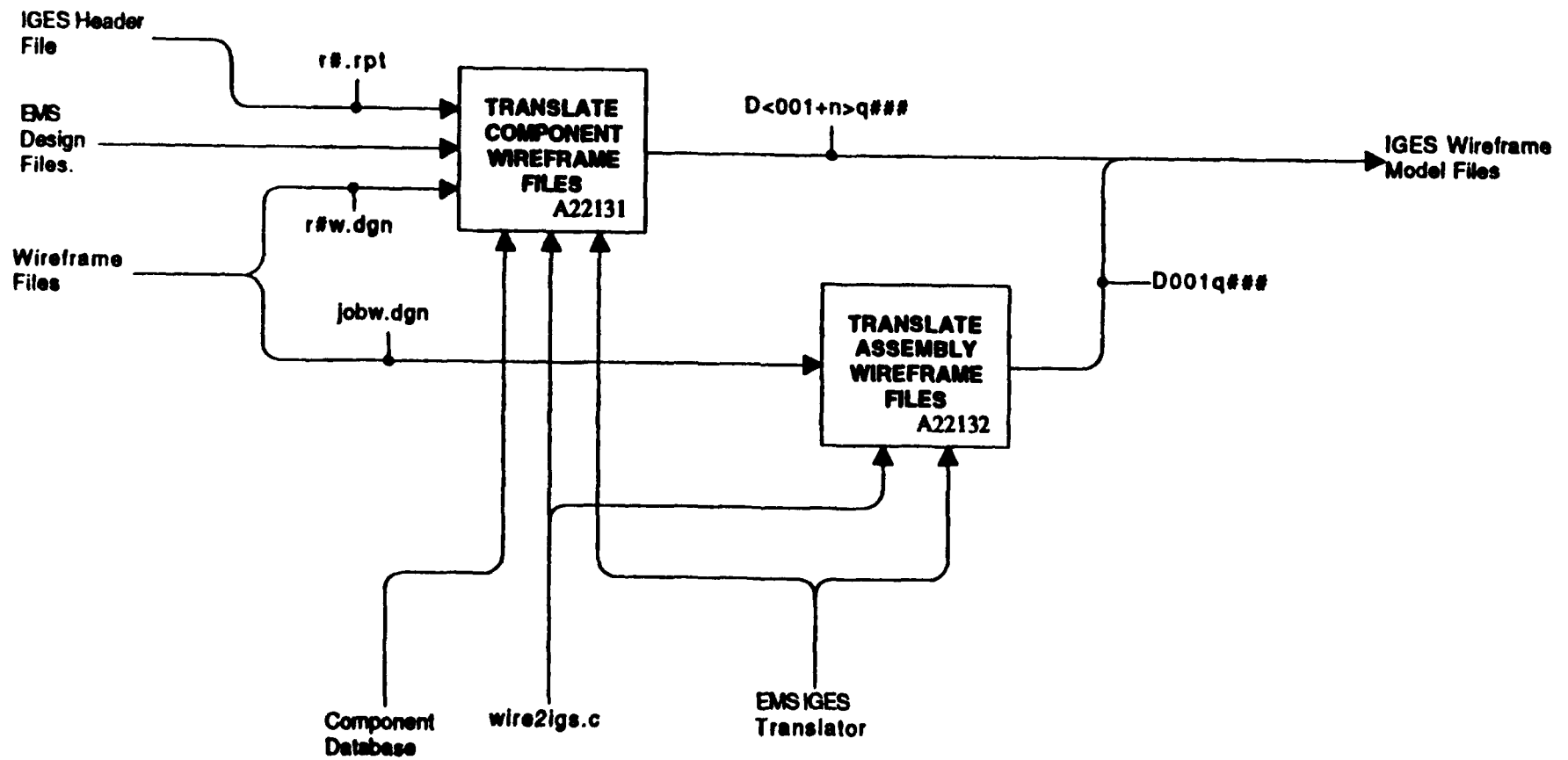
NODE: A2211	TITLE: TRANSLATE SOLIDS IGES FILES	NUMBER:

USED AT:	AUTHOR: Rob Fletcher	DATE: 4/7/92	X	WORKING	READER DATE	CONTEXT:
RAMP	PROJECT: RAMP Product Data Translation System (RPTS) for Printed Wiring Assemblies (PWA)	REV: 2		DRAFT		
	NOTES: 1 2 3 4 5 6 7 8 9 10			RECOMMENDED		
				PUBLICATION		



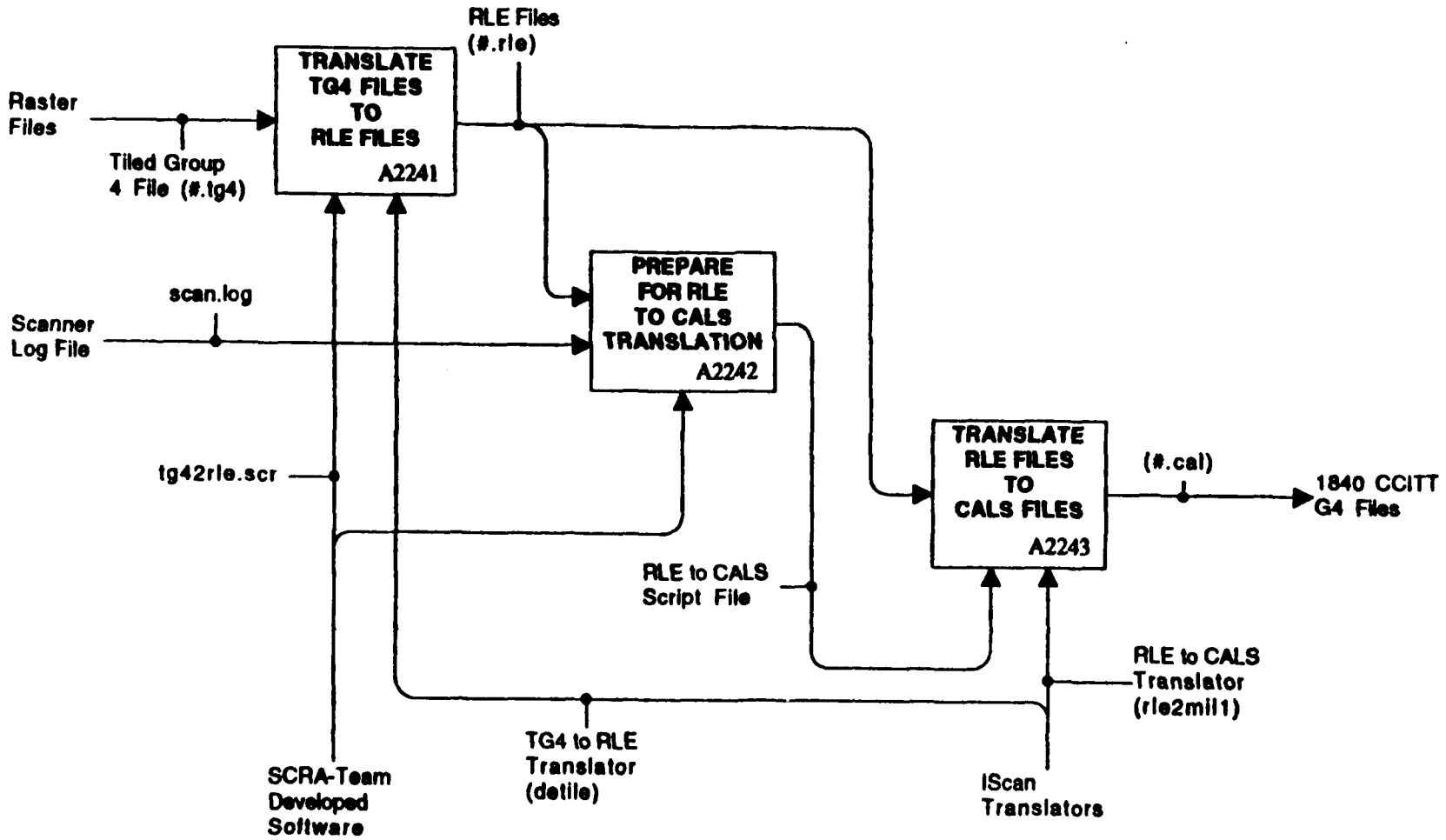
NODE: A2212	TITLE: TRANSLATE SURFACE IGES FILES	NUMBER:

USED AT:	AUTHOR: Rob Fletcher	DATE: 4/7/92	X	WORKING	READER DATE	CONTEXT:
RAMP	PROJECT: RAMP Product Data Translation System (RPTS) for Printed Wiring Assemblies (PWA)	REV: 2		DRAFT		
	NOTES: 1 2 3 4 5 6 7 8 9 10			RECOMMENDED		
				PUBLICATION		



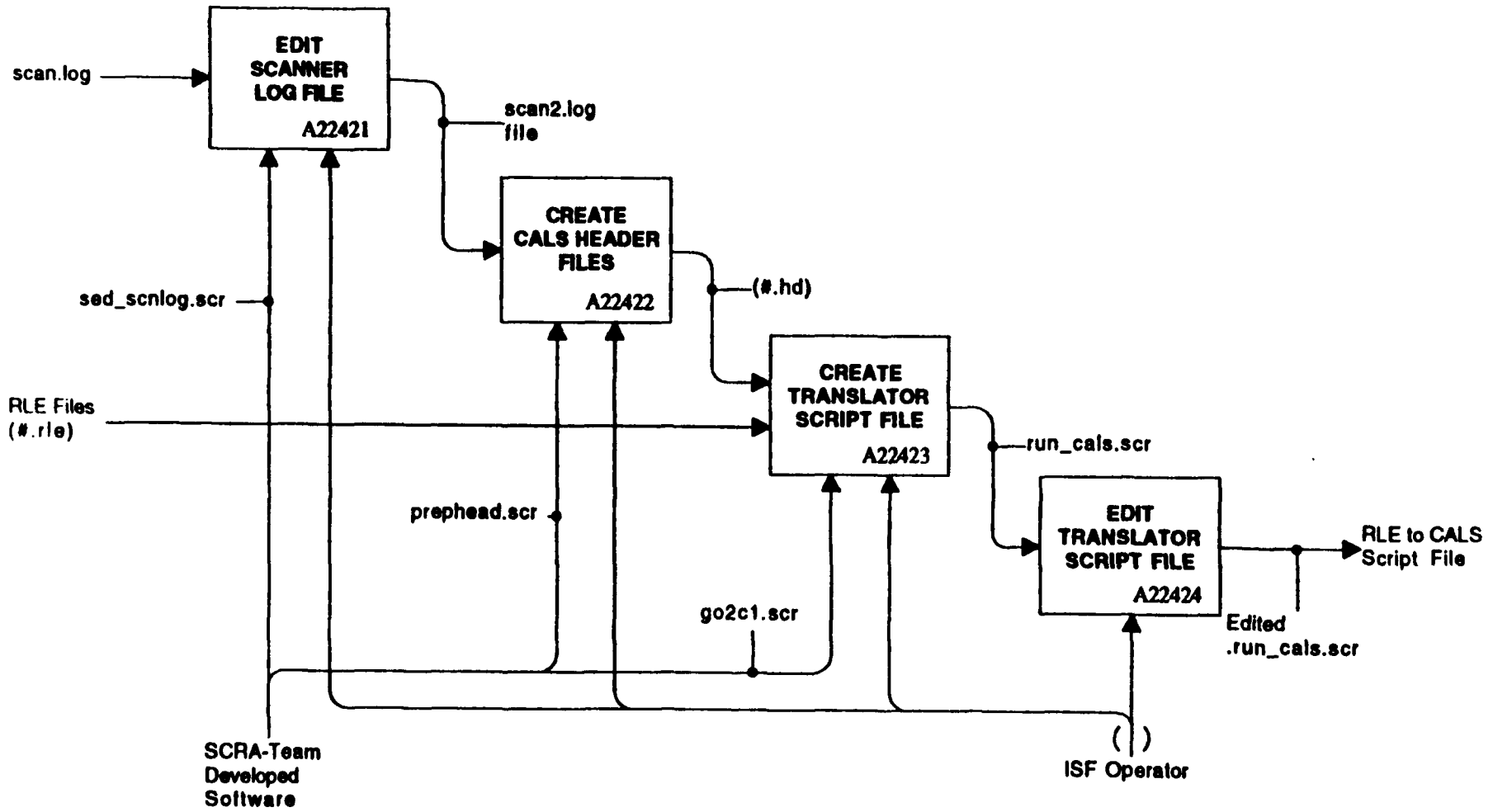
NODE: A2213	TITLE: TRANSLATE WIREFRAME IGES FILES	NUMBER:

USED AT:	AUTHOR: Rob Fletcher	DATE: 4/7/92	X	WORKING	READER DATE	CONTEXT:
RAMP	PROJECT: RAMP Product Data Translation System (RPTS) for Printed Wiring Assemblies (PWA)	REV: 2		DRAFT		
	NOTES: 1 2 3 4 5 6 7 8 9 10			RECOMMENDED		
				PUBLICATION		



NODE: A224	TITLE: GENERATE 1840 CCITT G4 FILES	NUMBER:

USED AT:	AUTHOR: Rob Fletcher	DATE: 4/7/92	X	WORKING	READER DATE	CONTEXT:
RAMP	PROJECT: RAMP Product Data Translation System (RPTS) for Printed Wiring Assemblies (PWA)	REV: 2		DRAFT		
	NOTES: 1 2 3 4 5 6 7 8 9 10			RECOMMENDED		
				PUBLICATION		



NODE: A2242	TITLE: PREPARE FOR RLE TO CALS TRANSLATION	NUMBER:

RPTS PWA Activity Model Glossary

The following glossary contains the terms used in the IDEF0 Activity Model for the RAMP Product Data Translation System for Printed Wiring Assembly. Low-level file names shown in the model may not be included in the glossary.

1840 CCITT G4 Files (Output)
The 1840 formatted CCITT G4 Files are raster files of the Technical Data Package (TDP) produced by the Intergraph scanner translators and 1840 software.

1840 EDIF File (Output)
The 1840 formatted EDIF File contains schematic information and is generated by the Intergraph Design Engineer EDIF 2 0 0 translator and 1840 software.

1840 IGES Files (Output)
The 1840 formatted IGES Files contain surface, solid, and wireframe representations of the PWA and components and are generated by the Intergraph Engineering Modeling System (EMS) IGES translator and 1840 software.

1840 Industry Standard Files (Output)
The 1840 Industry Standard Files are the EDIF, IGES, IPC, and CCITT G4 files formatted into Mil-Std-1840 format.

1840 IPC File (Output)
The 1840 formatted IPC File contains the PWB information and is generated by the Intergraph PCB Engineer IPC-D-350 translator and 1840 software.

2D PCB Data (Output)
The 2D PCB Data is the PCB Engineer design file containing the 2D representation of the PCB.

3D Component Model (Output)
The 3D Component Model is the design file(s) generated by the Intergraph EMS application.

Add Simulation Setup Data (Activity)
In the Add Simulation Setup Data process the operator sets up the simulation waveforms time/voltage window parameters.

Analog Analysis Tools (Mechanism)
The Analog Analysis Tools are COTS programs which run in conjunction with the Design Engineer schematic software to allow the operator to create CSPICE format netlists.

Annotation Values (Input)
The Annotation Values are the text and numerical information associated with a schematic symbol.

Aperture Card Scanner/Reader (Mechanism)
The Aperture Card Scanner/Reader is a system which reads aperture cards. The system reads the holerith code from the card and scans the film section of the card.

Aperture Card TDP (Input)

The Aperture Card TDP is TDP data which is input by aperture card.

Artwork Capture System (Mechanism)
The Artwork Capture System is a subsystem of the RPTS PWA. It is a

Artwork Capture PC AT (Mechanism)
The Artwork Capture PC AT is the PC which is used in conjunction with the paper TDP scanner.

Assemble Intelligent Data (Activity)
The Assemble Intelligent Data process takes the component data inputs and uses them to "look up" the related data in the RPTS databases. The process continues to capture raw data, but adds intelligence by creating data structures. For example, a component part number is linked to the component simulation model, physical description, specifications, etc.

Bill of Materials File (Output)
The Bill of Materials (BOM) File is generated from the data in the relational database and contains the data found on the TDP Bill of Materials.

BOM/Component Entry Program (Mechanism)
The BOM/Component Entry Program is the Oracle database program(s) which capture TDP Bill of Material and additional component data using operator input screens.

BOM Operator (Mechanism)
The BOM Operator is the operator trained to input the BOM data.

BOM Raster File (Input)
The BOM Raster File is used by the operator to enter the item number, item quantity, reference designator, and part number into the BOM database

Build Component Cells (Activity)
The Build Component Cells process utilizes the LOCPAD program, PCB Engineer Create Cell Function, and BOM information to produce a 2D component footprint (cell).

CALS 1840 File Set (Input)
The CALS 1840 File Set is the EDIF, IPC, IGES, and CCITT G4 files in Mil-Std-1840 format.

Capture 3D Models (Activity)
The Capture 3D Models process uses the Intergraph Engineering Modeling System to create 3D models of the PWA components and PWA. These models are later translated to IGES surface, solid, and wireframe files for each.

Capture Aperture Card data (Activity)
The Capture Aperture Card data process uses the Aperture Card Reader/Scanner to produce Tiled Group 4 raster files of the film images. The holerith data is also read from the cards and placed in a text file for downstream processing.

Capture Bom Line Items (Activity)
The Capture Bom Line Items process captures the item number, item quantity, reference designator, and part number into the BOM database.

Capture Component Data (Activity)

The Capture Component Data process gathers data such as component electrical values (5 volts, etc.), component physical parameters (length, width, etc.), and military/commercial component specifications. This data is distinguished from intelligent data because it consist primarily of text strings. In this process, none of the linking to related data is performed. The linking of this data is performed in the Assemble Intelligent Data process.

Capture/ Conversion Status Update (Input/Output)

The Capture/ Conversion Status Update is the operator's update of the system status when a process is complete.

Capture Define Waveform Net Names (Activity)

The Capture Define Waveform Net Names process defines the net names which are required for resetting devices to known conditions for simulation. This is required to assist the operator in debugging the PWA.

Capture Input Waveforms (Activity)

The Capture Input Waveforms process collects the board-level input waveforms from the raster TDP input waveform specifications.

Capture PCB Data (Activity)

The Capture PCB Data process is the top level process for capturing all the PCB data. This process uses PCB Engineer for capturing the 2D PCB data. This data is later converted to an IFC-D-350 file.

Capture Physical Attributes (Activity)

The Capture Physical Attributes process is the top level process for capturing all the 2D and 3D physical data of the PWA.

Capture Schematic Connectivity (Activity)

In the Capture Schematic Connectivity process the operator wires together the symbols according to the TDP schematic.

Capture Schematic Symbols (Activity)

The Capture Schematic Symbols process uses the Design Engineer environment to build the graphical schematic symbol from the Design Engineer Symbol Library , Component Library, TDP schematic, or IHS library.

Capture Schematic Symbol Data (Activity)

The Capture Schematic Symbol Data process is the top level process for capturing all schematic symbol data.

Capture Schematic (Activity)

The Capture Schematic process is the top level process for capturing all data related to the schematic. The primary software used is Design Engineer.

Capture Simulation Models (Activity)

The Capture Simulation Models process collects the models from the component library if they exist, or the operator writes the models from the specifications.

Capture Status (Output)

The Capture Status output is the operator's updating of the capture/conversion status table.

Capture Support Data (Input/Output)

The Capture Support Data is TDP administrative data generated for used in the translators. Most of this data is used to generate the 1840 declaration file.

Capture Symbol Annotation Values (Activity)

The Capture Symbol Annotation Values process adds annotation to the graphical symbols to produce a complete schematic symbol.

Capture TDP Images (Activity)

The Capture TDP Images process is the top level process for capturing the TDP images from paper, cards, or optical media.

Capture Technical Data (Activity)

The Capture Technical Data is the top level process for capturing the TDP data.

Capture Test Requirements (Activity)

The Capture Test Requirements is the top level process for capturing all the TDP board-level test requirements.

Captured TDP Data (Output)

The Captured TDP Data is the top level description of all the data captured for the TDP.

CCITT Files (Input/Output)

The CCITT Files are standard raster files.

Compare Schematic/PCB Connectivity (Activity)

The Compare Schematic/PCB Connectivity process performs a comparison of the schematic netlist with the PCB layout netlist for discrepancies between them. The errors are highlighted on the screen where the operator can correct them.

Component Cells (Output)

The Component Cells are the 2D footprints of the components on the PCB.

Component Data Capture Status (Output)

The Component Data Capture Status is the operator's update of the capture/conversion status table.

Component Data (Output)

The Component Data is the top level description of all the BOM and component data collected in the Capture Component Data process.

Component Database (Mechanism)

The Component Database is an Oracle relational database system populated with PWA component data.

Component Database Data (Input)

The Component Database Data consists of all BOM data, component footprints (cells), and schematic symbol data.

Component Parameters (Output)

The Component Parameters are the component specifications data which are linked to the BOM data for the component.

Convert Data To Native Format (Activity)

The Convert Data To Native Format process converts gerber (vector) files to PCB Engineer data.

Correct PCB Layout Notice (Output)

The Correct PCB Layout Notice is the detection of an error in the PCB layout found in the Compare Schematic/PCB Connectivity process. This allows the operator to go back an correct the PCB Engineer PCB data.

Correct Schematic Notice (Output)

The Correct Schematic Notice is the detection of an error found in the Verify Waveforms process. This allows the operator to go back and correct the schematic.

Cost/Delivery Estimate (Output)

The Cost/Delivery Estimate is a report sent to the customer for approval to proceed with the RPTS Order.

COTS Applications (Mechanism)

A COTS (Commercial Off The Shelf) Application is any of the vendor supplied software which is run on the system

Create Cals Header Files (Activity)

The Create Cals Header Files process generates the 1840 header data for the raster files.

Create Translator Script File (Activity)

The Create Translator Script File process is currently being updated to a C program.

Customer Approvals (Control)

The Customer Approvals is the report sent to the system which allows/disallows the system to continue with the order.

Customer Time Constraints (Control)

The Customer Time Constraints ICOM represents one of the primary controls of the system, i.e., to produce an 1840 file set within the time allowed for the job.

D001q### (Output)

The D001q### is the filename of the 1840 IGES file for item number ### within the 1840 document.

Data Availability (Control)

The Data Availability is a control of the system because incoming TDP's may have components specifications which cannot be located in the TDP itself or any of the system's libraries.

Data Not Found (Output)

The Data Not Found is self explanatory.

Declaration File (Output)

The Declaration File is an 1840 format file which lists all the files contained in the 1840 fileset. It also contains originating/destination system and other administrative data.

Design Engineer Symbol Library (Mechanism)
The Design Engineer Symbol Library is an Intergraph library containing schematic symbols.

Design Engineer (Mechanism)
The Design Engineer COTS software is the Computer Aided Engineering (CAE) tool for schematic capture work.

Design Engineer Data (Output)
The Design Engineer Data output represents all files generated by Design Engineer.

Digital/Analog Waveform Editors (Mechanism)
The Digital/Analog Waveform Editors are the programs which run in conjunction with Design Engineer to allow operator entry and editing of waveforms for simulation.

EDIF File (Input/Output)
The EDIF File contains schematic information and is generated by the Intergraph Design Engineer EDIF 2 0 0 translator.

EDIF Translator (Mechanism)
The EDIF Translator translates Design Engineer schematic design files into EDIF 2 0 0 format. The translator has read/write capability.

Edit Scanner Log File (Activity)
The Edit Scanner Log File process prepares the scanner log file for conversion to 1840 header files.

EDMICS Data (Input)
The EDMICS Data is the Navy Engineering Data Management Information Control System formatted Technical Data Package. The medium is optical disk.

Electrical Parameters File (Input)
The Electrical Parameters File contains data from the component database pertinent to the Capture Schematic process.

EMS (Mechanism)
The EMS mechanism is the Intergraph Engineering Modeling System. This is a 3D design and drafting system which enables the operator to create solid, surface, and wireframe models of the PWA and components.

EMS Data (Output)
The EMS Data output represents EMS design files and all other outputs of EMS.

EMS Design Files. (Input)
The EMS Design Files are the solid, surface, and wireframe model files of the PWA and components. These files are later translated by the IGES translator.

EMS IGES Translator (Mechanism)
The EMS IGES Translator translates EMS 3D design files into IGES format. The translator has read/write capability.

External Reports (Output)
An External Report is any ad hoc hard-copy report produced by the system.

Flatbed Scanner (Mechanism)
The Flatbed Scanner is an HP scanner used to read paper TDPs.

Generate 1840 EDIF File (Activity)
The Generate 1840 EDIF File is the process in which the EDIF translator is run and the output file is reformatted to the 1840 standard.

Generate 1840 IGES Files (Activity)
The Generate 1840 IGES Files is the process in which the IGES translator is run and the output file is reformatted to the 1840 standard.

Generate 1840 CCITT G4 files (Activity)
The Generate 1840 CCITT G4 files is the process in which the Artwork Capture system translators are run and the output files are reformatted to the 1840 standard.

Generate 1840 IPC File (Activity)
The Generate 1840 IPC File is the process in which the IPC translator is run and the output file is reformatted to the 1840 standard.

Generate Declaration file (Activity)
The Generate declaration file process generates an 1840 declaration file for the PWA.

Generate MIL-STD-1840 Industry Standard Files (Activity)
The Generate MIL-STD-1840 Industry Standard Files is the top level process which performs all of the translations required to generate the 1840 document (fileset).

Generate Netlist (Activity)
The Generate Netlist process is performed by the Design Engineer I/O Utility to generate a schematic netlist.

Gerber Data Reader (Mechanism)
The Gerber Data Reader is a function of PCB Engineer which reads the data into the PCB Engineer native format.

Hilo (Mechanism)
The Hilo mechanism is the CAE digital simulator used for verifying schematic capture of digital circuits.

IEEE Schematic Symbol Graphics (Output)
The IEEE Schematic Symbol Graphics are the standard graphical symbols used to create schematic symbols.

IGES File (Input/Output)
The IGES Files contain surface, solid, and wireframe representations of the PWA and components and are generated by the Intergraph Engineering Modeling System (EMS) IGES translator.

IGES Header File (Input)
The IGES Header File is the section of the IGES file containing 1840 format information.

IGES Pre-Start Section File (Input)

The IGES Pre-Start Section File is a section of the IGES file where data not able to be placed in the standard IGES format (due to translator deficiencies) is placed. This data is formatted according to the RPTS PWA Product Data Description Document.

IGES Solid Model Files (Output)

The IGES Solid Model Files contain the EMS 3D solid representations of the PWA and components.

IGES Surface Model Files (Output)

The IGES Surface Model Files contain the EMS 3D surface representations of the PWA and components.

IGES Wireframe Model Files (Output)

The IGES Wireframe Model Files contain the EMS 3D wireframe representations of the PWA and components.

IHS Operator (Mechanism)

The IHS Operator is the operator trained to use the IHS system.

IHS System (Mechanism)

The IHS System is a CD-ROM based library of PWA data. This library provides access to military and federal specifications and standards, commercial standards for integrated circuits and discrete semiconductors, and a vendor master directory containing vendor names, addresses, etc.

Input Waveform Specifications (Input)

The Input Waveform Specifications are the raster test specifications which are read by the test operator and entered into the system.

Input Waveforms (Output)

The Input Waveforms are the test waveforms captured for use in simulation.

Instantiated Annotated Symbol (Output)

The Instantiated Annotated Symbol output is the schematic symbol with its associated reference designator and other annotation for the PWA.

Intelligent Data Capture Status (Output)

The Intelligent Data Capture Status is the top level ICOM for all status updates within the process.

Intergraph CAE System (Mechanism)

The Intergraph CAE System is a network configuration of a UNIX-based Computer Aided Engineering Workstations.

IPC-D-350 File (Input/Output)

The IPC-D-350 File contains the PWB information and is generated by the Intergraph PCB Engineer IPC-D-350 translator.

IPC Translator (Mechanism)

The IPC Translator translates PCB Engineer 2D design files into IPC-D-350 format. The

translator has read/write capability.

IScan (Mechanism)
The IScan mechanism is the set of raster utilities which allow raster image viewing and translation between different formats.

IScan Translators (Mechanism)
The IScan Translators are the translators found in the IScan raster utilities.

ISF Input Status (Output)
The ISF Input Status is the operator update of the capture/conversion table to reflect the status of the reading the ISFs.

ISim (Mechanism)
The ISim mechanism is an Intergraph mixed-mode simulator for verifying schematic capture.

Locate Specification (Activity)
The Locate Specification process is represents the search performed on the RPTS libraries for component data.

LOCPAD Program (Mechanism)
The LOCPAD Program is a C program which uses the MicroCSL procedural interface to PCB Engineer to assist the operator in building the 2D component footprints.

Order Status (Output)
The Order Status is a state table containing the states of various processes in the system.

Output Waveform Specifications (Input)
The Output Waveform Specifications are the raster test specifications which are read by the test operator and entered into the system.

Output Waveforms (Output)
The Output Waveforms are the test waveforms captured for use in simulation.

Paper TDP (Input)
The Paper TDP is a Technical Data Package received on paper media.

Part Number (Input/Output)
The Part Number is that of the component found on the TDP Bill of Materials.

PCB Engineer (Mechanism)
The PCB Engineer mechanism is a CAE application for capturing printed circuit board design data.

PCB Engineer Data (Input/Output)
The PCB Engineer Data is the 2D representation of the PCB.

PCB Engineer Library (Mechanism)
The PCB Engineer Library contains the PCB footprints, or component cells, for use in capturing the PCB data.

Perform Common Functions (Activity)

The Perform RPTS Common Functions activity shows all of the processes which are common to any RPTS. The system is designed to be modular to allow other functions to replace the RPTS PWA Functions. This decomposition of this process is incomplete at the time of this publication.

Perform PWA Functions (Activity)

The Perform PWA Functions activity is the top level process of all the PWA processing. The system is designed to allow this module to be removed and replaced with other functions creating a new RPTS system.

PERFORM RPTS PWA FUNCTIONS (Activity)

This is the top level process representing all functionality of the system and showing all external ICOMs.

Pin/Pad Table (Output)

The Pin/Pad Table is a file containing a list of the pin identifications and the associated pad geometries.

Place And Label Symbols (Activity)

In the Place And Label Symbols process the operator runs the Place Symbols program to automatically place and label the schematic symbols.

Place Component Cells (Activity)

In the Place Component Cells process the operator takes the 2D component cells (footprints) and places them on the PWB.

Place Symbols Program (Mechanism)

The Place Symbols Program is C program used to place and label the schematic symbols.

Place Symbols Program (pl_symbol.cmd) (Mechanism)

The Place Symbols Program is a C program which allows the operator to place all the pre-generated and instantiated (includes reference designator) schematic symbols on the Design Engineer schematic capture screen at once. The prevents the operator from having to go to the database for each symbol.

Placed and Labeled Symbols (Output)

The Placed and Labeled Symbols are the schematic symbols which have already been placed on the schematic and are ready to be wired together.

Prepare For RLE To CALS Translation (Activity)

Currently being replaced by a C program which will change this part of the model.

prephead.scr (Mechanism)

The prephead.scr is currently being replaced by a C program which will change this part of the model.

Raster Artwork Files (Input)

The Raster Artwork Files are the scanned paper or film artwork files.

Raster Data Capture Status (Output)

The Raster Data Capture Status is the operator update of the capture/conversion status table.

Raster Files (Output)
The Raster Files output represents all scanned output raster files in the system.

Raster Schematic Files (Input)
The Raster Schematic Files are the scanned schematic data files.

Raster Test Requirements Files (Input)
The Raster Test Requirements Files are the scanned test requirements data files.

Read 1840 Status (Output)
The Read 1840 Status is the operator update of the capture/conversion status table for the Read CALS 1840 Document process.

Read CCITT Status (Output)
The Read CCITT Status is the operator update of the capture/conversion status table for the Read CCITT File process.

Read EDIF Status (Output)
The Read EDIF Status is the operator update of the capture/conversion status table for the Read EDIF File process.

Read IGES Status (Output)
The Read IGES Status is the operator update of the capture/conversion status table for the Read IGES File process.

Read 1840 Industry Standard Files (Activity)
The Read Industry Standard Files process is the top level process for reading each file of the 1840 formatted fileset.

Read IPC Status (Output)
The Read IPC Status is the operator update of the capture/conversion status table for the Read IPC File process.

Read CALS 1840 Document (Activity)
The Read CALS 1840 Document is the process which reads an 1840 formatted tape, strips the 1840 headers, translates the files, and sends them to the proper directories.

Read CCITT File (Activity)
The Read CCITT File process is the translation of the CCITT G4 files to native format.

Read EDIF File (Activity)
The Read EDIF File process is the translation of the EDIF files to native format.

Read EDMICS Data (Activity)
The Read EDMICS Data process reads an EDMICS optical disk based TDP. This activity is currently not implemented.

Read IGES File (Activity)
The Read IGES File process is the translation of the IGES files to native format.

Read IPC File (Activity)
The Read IPC File process is the translation of the IPC files to native format.

Reference Designators (Input)
Reference Designators are the annotations used to identify schematic symbols and PCB footprints.

Relational Database (Mechanism)
The Relational Database is the Oracle Relation DataBase System.

Required Waveforms List (Output)
The Required Waveforms List identifies those schematic net which require waveforms be defined for simulation.

RLE to CALS Translator (rle2mil1) (Mechanism)
The RLE to CALS Translator converts Run Length Encoded raster files to CALS Group 1 raster files.

RLE to CALS Script File (Output)
The RLE to CALS Script File is currently being rewritten into a C program which will change this part of the model.

RPTS Order (Input)
The RPTS Order is a request from the customer for the system to process a Technical Data Package. The TDP must accompany the order.

Scan Paper TDP (Activity)
The Scan Paper TDP process uses the HP paper scanner and IScan software to convert paper TDP drawings to raster images.

Scanner Log File (Input)
The Scanner Log File is generated by the Artwork Capture System and contains a record identifying each raster file.

Schematic (Output)
The Schematic output is the Design Engineer design file for translation to EDIF.

Schematic-Symbol Graphics Building Blocks (Input)
The Schematic-Symbol Graphics Building Blocks are the primitive symbols used to build a standard IEEE schematic symbol.

Schematic Netlist File (Input)
The Schematic Netlist File is the node list from the schematic showing all component pin locations per node.

Schematic Symbol Files (Output)
The Schematic Symbol Files contain the complete annotated schematic symbols for the PWA.

SCRA-Team Developed Software (Mechanism)
The SCRA-Team Developed Software is software which was developed in-house as opposed to Commercial Off The Shelf (COTS) software.

Search CD-ROM Database (Activity)

The Search CD-ROM Database is the process of using the IHS CD-ROM system to look up the commercial,military, and federal specifications and standards.

Search Component Table (Activity)

The Search Component Table process allows the operator to pull up the component table of the component database information for entry into the current process.

Search Form Factor Table (Activity)

The Search Form Factor Table process allows the operator to pull up the form factor table of the component database information for entry into the current process.

Simulate Circuit (Activity)

The Simulate Circuit process applies the captured input waveforms to the Intergraph ISim or Hilo simulators to generate the expected output waveforms.

Simulation Model Specification (Input)

The Simulation Model Specification is the data found in the raster test requirements files specifically pertaining to simulation input.

Simulation Models (Output)

The Simulation Models are the component models built or retrieved by the test operator for use in simulation.

Simulation Parameters File (Input)

The Simulation Parameters File is a file containing a simulation model from the component database. This is data which was saved for a particular component from a previous job of the RPTS.

Simulation Waveform Names (Output)

The Simulation Waveform Names are the names applied to the nets by the operator for use in simulation. These names are more meaningful to the operator that the generic names applied by the system.

Solids Files (Input)

The Solids Files are EMS solid model design files for subsequent translation to IGES.

Support Files (Output)

The Support Files output is a representation of the administrative and other data required downstream for ISF translation.

Surface Files (Input)

The Surface Files are EMS surface model design files for subsequent translation to IGES.

Symbol Identifiers (Input)

The Symbol Identifiers are the specific schematic symbol data the operator looks for in the TDP schematic when performing schematic capture.

System Availability (Control)

The System Availability ICOM shows that a major controlling factor of the system is how many workstations are available at a time. Another factor is whether the desired application is found

on the available workstation.

System Waveform Names Per Net (Input)
The System Waveform Names Per Net are the names assigned to the nets by the system.

TDP Capture Conversion Status (Output)
The TDP Capture Conversion Status is provided to the operator to allow him to see what processes have been completed for an order.

TDP Data Archive File (Output)
The TDP Data Archive File is a file containing all data captured in the system for a particular PWA.

Technical Data Package (TDP) (Input)
The Technical Data Package (TDP) is a complete level 3 data package. TDP's in paper, film, aperture cards, or RAMP compatible product data files, or combinations of these can b accepted.

Technical Data Deficiency Report (Output)
The Technical Data Deficiency Report is a report of a deficiency in the TDP which is sent to the Cognizant Technical Authority for resolution before the RPTS job can continue.

TG4 to RLE Translator (detile) (Mechanism)
The TG4 to RLE Translator is an IScan utilities translator for translating Tiled Group 4 raster files to Run Length Encoded raster format.

Trained Operators (Mechanism)
The operators are trained on various applications of the Intergraph system. Operators are rotated from task to task based on their training.

Translate Assembly Solid Files (Activity)
The Translate Assembly Solid Files process translates the EMS solid model design files of the PWA to IGES.

Translate Assembly Surface Files (Activity)
The Translate Assembly Surface Files process translates the EMS surface model design files of the PWA to IGES.

Translate Assembly Wireframe Files (Activity)
The Translate Assembly Wireframe Files process translates the EMS wireframe model design files of the PWA to IGES.

Translate Component Solid Files (Activity)
The Translate Component Solid Files process translates the EMS solid model design files of the PWA components to IGES.

Translate Component Surface Files (Activity)
The Translate Component Surface Files process translates the EMS surface model design files of the PWA components to IGES.

Translate Component Wireframe Files (Activity)
The Translate Component Wireframe Files process translates the EMS wireframe model design

files of the PWA components to IGES.

Translate RLE Files To CALS Files (Activity)
The Translate RLE Files To CALS Files process uses the IScan utilities to translate Run Length Encoded raster files to CALS Group 1 raster files.

Translate Solids IGES Files (Activity)
The Translate Solids IGES Files process represents the translation of all the EMS solid model design files to IGES.

Translate Surface IGES Files (Activity)
The Translate Surface IGES Files process represents the translation of all the EMS surface model design files to IGES.

Translate TG4 Files To RLE Files (Activity)
The Translate TG4 Files To RLE Files process translates the Tiled Group 4 raster files to Run Length Encoded raster files.

Translate Wireframe IGES Files (Activity)
The Translate Wireframe IGES Files process represents the translation of all the EMS wireframe model design files to IGES.

Translated CCITT Data (Output)
The Translated CCITT Data output is the CCITT file which has been converted to native format.

Translated IPC Data (Output)
The Translated IPC Data is the IPC-D-350 file which has been converted to native format.

Translated Standards Data (Output)
The Translated Standards Data represents all standards input data to the system which has been translated to native format.

Translation Status (Output)
The Translation Status is represents the operator update of the capture/conversion status table for all translations.

Translator Input Data (Output)
The Translator Input Data represents all the captured CAE data for downstream translation to the 1840 fileset.

Verify Waveforms (Activity)
In the Verify Waveforms process the operator compares the output waveforms of the simulation to the TDP test specification output waveforms. If a discrepancy is found, the operator must check the schematic for errors.

VScan (Mechanism)
The VScan software converts raster files to vector (gerber) files.

Wireframe Files (Input)
The Wireframe Files are EMS wireframe model design files for subsequent translation to IGES.